楊富量博士 (Fu-Liang Yang, Ph. D.) 簡介

Director General and Research Fellow
National Nano Device Laboratories (NDL)
No. 26, Prosperity Road 1, Hsinchu Science Park,
Hsinchu 30078, Taiwan
Tel : 886-3-5726100 ext. 7701
Fax : 886-3-5735670
Email: flyang@ndl.narl.org.tw

EDUCATION

- Ph.D., Department of Materials Science and Metallurgy, University of Cambridge, UK, (*1991 – 1994)*
- B.S., Department of Materials Science and Engineering, National Tsing Hua University, (*1985 – 1989*)

PROFESSIONAL EXPERIENCE

- Director General, National Nano Device Laboratories (NDL) (*2008 ~ present)*
- Deputy Director, R & D TSMC; TSMC Acaedmician, TSMC Academy *(2000 ~ 2008)*
- Deputy Manager, Department of Device Development, Vanguard International Semiconductor Corporation (VIS) (*1994 ~ 2000)*
- 51th IC Industry Committee Member of The Chinese Institute of Electrical Engineering (*2009 ~ present)*
- Executive Director of 6th ROC (Taiwan) Nanotechnology and Micro System Association (*2009 ~2010)*
- Review Committee member of International Nanotechnology Exhibition & Conference (Nano Tech, alternatively held in Taiwan & Japan) *(2009~2010)*
- Review Committee member of Advance Memory Program by Science and Engineering Research Council (SERC), Singapore *(2009 and 2011)*
- Co-General Chair of Joint Workshop on Nano-Process and Nano-Device, Japan *(2010)*
- Program committee member of International Conference on Solid State Devices and Materials(SSDM), Japan *(2010~Present)*
- Review Committee Member of R & D Center in Taiwan Program, Department of Industrial Technology (DoIT), Ministry of Economic Affairs (MOEA), Taiwan (*2010~ present)*
- Technical committee member of International Electron and Device Meeting (IEDM), U.S.A *(2010~2011)*
- Director of 7th ROC (Taiwan) Nanotechnology and Micro System Association (*2011 ~ present)*
- Senior Advisor of National Program on Nano Technology (*2011~ present)*

RESEARCH SUMMARY

From 1994 to 2000, Dr. Fu-Liang YANG was with Vanguard International Semiconductor Corporation (VIS), where he worked on DRAM process and device development. From 2000 to 2006, he managed a department in Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, with research focuses on novel transistor architecture and process technologies for sub-32nm node logic and nonvolatile memory. Since January 2007, he has conducted a phase-change memory program for NAND/NOR Flash replacement in TSMC. He has authored or coauthored over 30 publications in IEDM, Symposium on VLSI Technology, and IEEE journals. He owns more than 100 patents in advanced CMOS devices and dynamic/static / nonvolatile memory technologies. One of his distinguished achievements is holding CMOS scaling record for gate length down to 5nm. This work published in 2004 has been cited 199 times. On August 1, 2008, he was inaugurated as Director General of National Nano Device Labortories (NDL) with research focuses on the emerging nanotechnologies, such as sub-20nm CMOS technology, new generation photovoltaic, and MEMS or Bio-MEMS. A recent achievement was forming the smallest 16nm functional SRAM cell by the innovative Nano-Injection Lithography (maskless and photoresist free), which has just been published as IEDM-2009 late news paper. In 2010, Dr. YANG led another research team achieving functional R-RAM cell array with half pitch down to 9nm.