Review and Outlook for Semiconductor Processing Technology

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CMOS technology has been on schedule advanced from 65nm, 45nm, to 32nm node production in 2005, 2007, and 2009, respectively, and 22nm production has also been realized in early 2012. The first 14nm production is now shown in roadmap in around 2014. This fast-trend scaling till 32nm node was on the basis of maintaining almost the same device structure but introducing one or two new materials on source/drain, gate dielectric, or gate, to compensate carrier mobility loss upon gate length scaling. Since 22nm the device structure has been greatly modified from "planar" to so-called "FinFET" for further alleviating short gate-length effects. In this talk, special attention will also be paid on relevant technologies for reducing power consumption and dealing with increasing electrical characteristic fluctuations.

Furthermore, TMO-RRAM (Transition-Metal-Oxide based Resistive Random Access Memory) is attractive and much investigated for emerging non-volatile memory recently, mainly due to its process simplicity and scalability. A CMOS compatible TMO system, WO_x by 450°C thermal oxidation, and special patterning technology of NInL (Nano Injection Lithography) technique are used to study sub-10nm scaling issues. We show for the first time that the decreasing trend of the I_{prog} of our TMO-RRAM accelerates below 20nm, and the smallest RRAM at 9nm half pitch. Its I_{prog} is only 1 μA and well below the expected current drive capability of the transistors. Such improvement in programming current is highly encouraging for future high-density RRAM production beyond NAND Flash.