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High-Performance Nanowire Electronics and Photonics on Glass and Plastic Substrates

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ABSTRACT

The merger of nanoscale building blocks with flexible and/or low cost substrates could enable the development of high-performance electronic and photonic devices with the potential to impact a broad spectrum of applications. Here we demonstrate that high-quality, single-crystal nanowires can be assembled onto inexpensive glass and flexible plastic substrates to create basic transistor and light-emitting diode devices. In our approach, the high-temperature synthesis of single-crystal nanowires is separated from ambient-temperature solution-based assembly to enable the fabrication of single-crystal-like devices on virtually any substrate. Silicon nanowire field-effect transistors were assembled on glass and plastic substrates and display device parameters rivaling those of single-crystal silicon and exceeding those of state-of-the-art amorphous silicon and organic transistors currently used for flexible electronics on plastic substrates. Nanowire transistor devices have been configured as low-threshold logic elements with gain; moreover, the high-performance characteristics are relatively unaffected by operation in a bent configuration or by repeated bending. The generality of this approach is further illustrated with the assembly of gallium nitride nanowire UV-light-emitting diodes on flexible plastic substrates. These results suggest that nanowires could serve as high-performance building blocks for the next of generation lightweight display, mobile computing, and information storage applications.

There is currently substantial interest in the fabrication of semiconductor devices on noncrystalline substrates such as plastics and glass because devices made on these low-cost and lightweight substrates serve as the basis for a large and rapidly growing class of electronics applications, including flat-panel displays, smart cards, and wearable displays.[1−5] For example, amorphous silicon can be deposited on glass at relatively low temperatures using vacuum deposition techniques and is used as the active component of transistors in flat-panel displays. The low carrier mobility[1,2,6] of amorphous silicon restricts its use to pixel-switching elements in these displays, thus requiring additional higher-performance electronics to drive the switching elements. These performance limitations can be overcome with polycrystalline silicon, which has demonstrated carrier mobilities approaching that of single-crystal silicon,[7] thereby opening up the possibility of combining pixel elements, display drivers, and more complex electronics on the display substrate. However, the additional steps and higher-temperature processing required to achieve high-quality polycrystalline silicon represent limitations in the implementation of polycrystalline silicon transistors on large-scale glass and plastic substrates.[3]

As an alternative to these silicon-based materials, there has also been substantial effort placed on utilizing organic materials as active semiconductor elements.[2,5] An attractive feature of organic semiconductors is the potential for room-temperature, solution-based processing that can be easily coupled to flexible plastic substrates.[8,9] Yet the low carrier mobilities exhibited by organic semiconductors,[2,10] which are comparable to or lower than those of amorphous silicon, restrict the potential function and corresponding applications possible with these materials. Overall, these results indicate a dichotomy in the capabilities of current materials—either low performance and broad substrate applicability (organics and amorphous silicon) or high performance and restricted substrate use (polycrystalline silicon)—which if overcome could open up exciting opportunities such as the integration of high-performance multifunctional electronics and displays on flexible plastics.

Here, we describe a new approach to this general problem that utilizes the solution-based assembly of high-performance inorganic semiconductor nanowire (NW) devices, where the functional properties are defined by NW building blocks used

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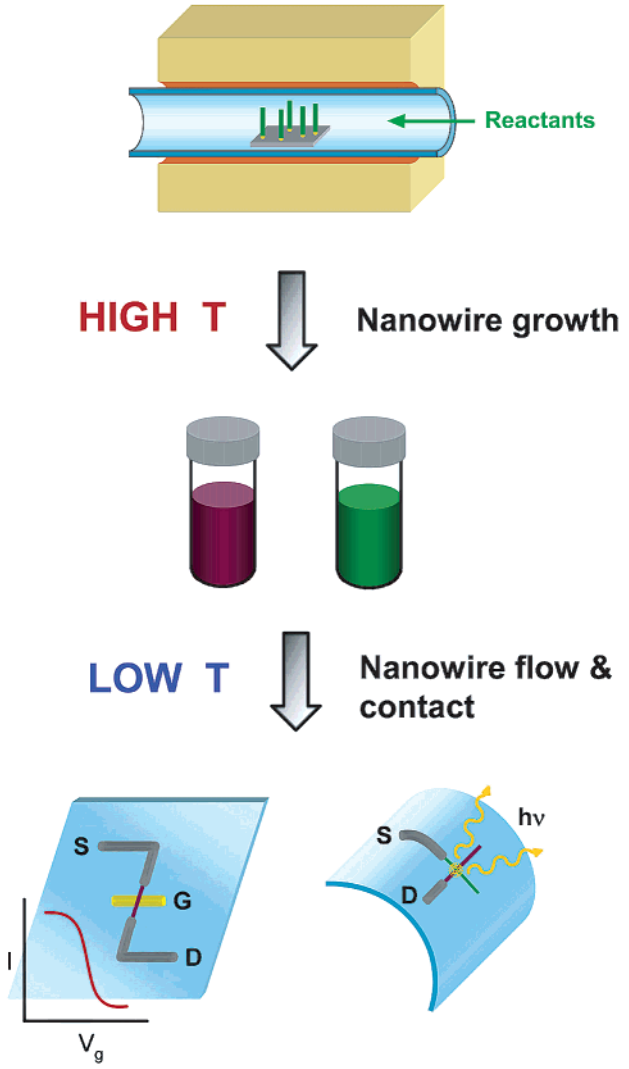

Figure 1. NW growth and device assembly on glass and plastic substrates. High-quality NWs of desired composition (purple, green) are prepared in a high-temperature process and subsequently dispersed into solution. Solution-based assembly then yields devices with diverse functionalities.

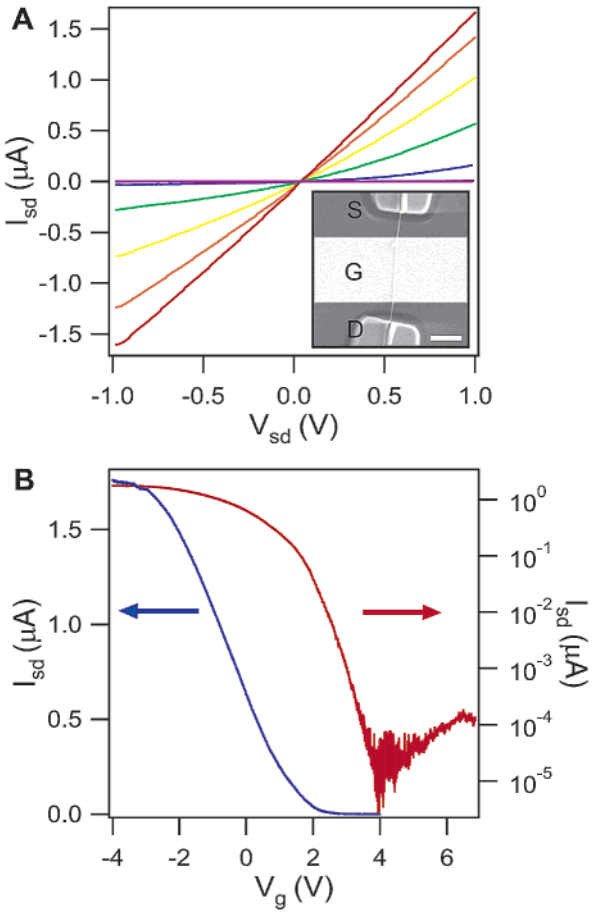

Figure 2. NW device characterization on glass substrates. (A) I_{sd} vs V_{sd} curves for a 20-nm p-SiNW FET on glass. The red, orange, yellow, green, blue, and purple curves correspond to $V_g = -3$, -2, -1, 0, 1, and 2 V, respectively. (Inset) Scanning electron microscopy (SEM) image of the device. The source (S), drain (D), and gate (G) are labeled. The scale bar is 1 μm. (B) I_{sd} versus V_g ($V_{sd} = 1$ V) for the device shown in A, plotted on a linear scale (left axis, blue curve) and log scale (right axis, red curve). The log-scale plot consists of two curves recorded at two sensitivities and joined for clarity.

in the assembly process.[11] There are three key features of our approach (Figure 1). First, the synthesis of NW building blocks is carried out under conditions optimized to yield high-quality single-crystal materials, where the desired electronic and/or photonic functions are defined by material composition, structure, and diameter.[12] Because this growth phase is independent of the stage in which active devices are fabricated, there is no need to be concerned with thermal and other substrate limitations, in contrast to direct thin-film deposition. In addition, previous characterization studies carried out on single-crystal substrates have shown that NWs of silicon,[13−15] gallium nitride,[15−17] and other materials[18−20] can exhibit properties comparable to the best bulk and epitaxial single-crystal semiconductors.[13] Second, the NWs can be readily isolated as stable solution suspensions that are then used for the deposition and patterning of devices.[21] The use of NW suspensions has the same processing advantages as the use of organic semiconductors[8,9] and also enables us, via the sequential transfer of distinct NWs, to introduce very different types of functions on the same substrate. Third, high aspect ratio NWs can be interconnected without the need for advanced lithography; that is, this approach takes advantage of the unique properties and processability of these nanoscale materials but does not require us to make ultrasmall devices to achieve high performance.

We first illustrate this approach with the assembly of p-type silicon NW field-effect transistors (p-SiNW FETs)[13−15] on glass substrates. The key steps in the overall device fabrication process[22] included (i) patterning of gate electrodes on the glass substrate, (ii) fluid-directed assembly[21] of the NWs across the gate electrodes, and (iii) lithography and metallization to form source-drain contacts to the NWs. The gate dielectric used in these experiments was either a ca. 2-nm-thick shell of SiO_2 surrounding the SiNWs[18,23] or a 20-nm-thick layer of SiO_2 deposited on the gate electrodes prior to NW assembly. Representative current versus source-drain voltage (I_{sd} versus V_{sd}) data (Figure 2a) recorded for different values of the gate voltage (V_g) exhibit a linear

response. This linear response shows that contacts behave in a practical sense as ohmic, suggesting that contacts can be made on glass substrates.

Key characteristics of these NW FETs were determined from I_{sd} versus V_g data (Figure 2b). The p-SiNW devices exhibit relatively large on currents of a ca. microampere (V_{sd} = 1 V). The transconductance, dI_{sd}/dV_g, that is obtained from the linear portion of the data has a value of 460 nA V^{-1} for the device shown and yields[24] a hole mobility of 365 cm^2 V^{-1} s^{-1}. Notably, the hole mobility value is comparable to or larger than that observed in single-crystal p-type silicon.[25] An extension of this linear region yields a threshold voltage of 1.7 V. In addition, an examination of the full I_{sd} versus V_g curve shows an on/off ratio of $\sim 10^5$ and a subthreshold slope of 550 mV per decade change in current.

A similar approach was used to assemble p-SiNW FETs on flexible plastic substrates. Typical I_{sd} versus V_{sd} data (Figure 3a) recorded for different values of V_g exhibit a linear response and thus demonstrate that ohmic contacts to the SiNWs are achievable on the plastic substrates using post-NW synthesis processing performed entirely at room temperature. In addition, other important metrics of these NW transistors are comparable to those found on glass substrates. From I_{sd} versus V_g curves (Figure 3b), we obtain a transconductance value of 650 nA V^{-1} and a threshold voltage of 1 V. The corresponding mobility calculated for this device was 135 cm^2 V^{-1} s^{-1}. An analysis of the subthreshold region of these data further reveals an on/off ratio of 10^5 and a subthreshold slope of 175 mV per decade change in current. Overall, these results show that p-SiNW transistors assembled on plastic and glass substrates exhibit similar characteristics. The on current for the NW/plastic device shown (Figure 3b) is somewhat lower than that for the NW/glass structure (Figure 2b), although measurements of additional NW/plastic transistors showed values (1.2−2.5 μA) that are essentially the same.

These results for NW transistors obtained on glass and plastic substrates can be compared to values reported previously for amorphous silicon, polycrystalline silicon, and organic thin films deposited on glass and plastic substrates. First, the values of mobilities obtained for the SiNW/plastic and SiNW/glass devices are comparable to or better than the highest values reported for p-channel polycrystalline silicon transistors, $\sim$200 cm^2 V^{-1} s^{-1}, on nonalkali glass[7] and are at least 2 to 3 orders of magnitude larger than typical values observed for amorphous silicon and organic transistors on glass and plastic substrates.[6,10] This comparison with amorphous silicon and organic transistors is especially striking, and we believe that it most clearly indicates the potential of our approach for future applications on flexible plastics. To elaborate this point further, we also compare the threshold voltage (1−2 V) and subthreshold swing (175−550 mV dec^{-1}) for NW devices versus amorphous silicon[26−29] (1.5−4 V; 300−600 mV dec^{-1}) and organics[30−33] (1−10 V; 400−1600 mV dec^{-1}) on plastic and glass substrates. The lower values of these key parameters for the SiNW devices, which are similar to those reported for polycrystalline silicon transistors,[7,34,35] could offer advantages for low-power operation. The on/off current ratios of the NW devices reported here are lower than the best amorphous silicon transistor values, 10^6−10^8, on glass and plastic,[6,27,31,33] although recent

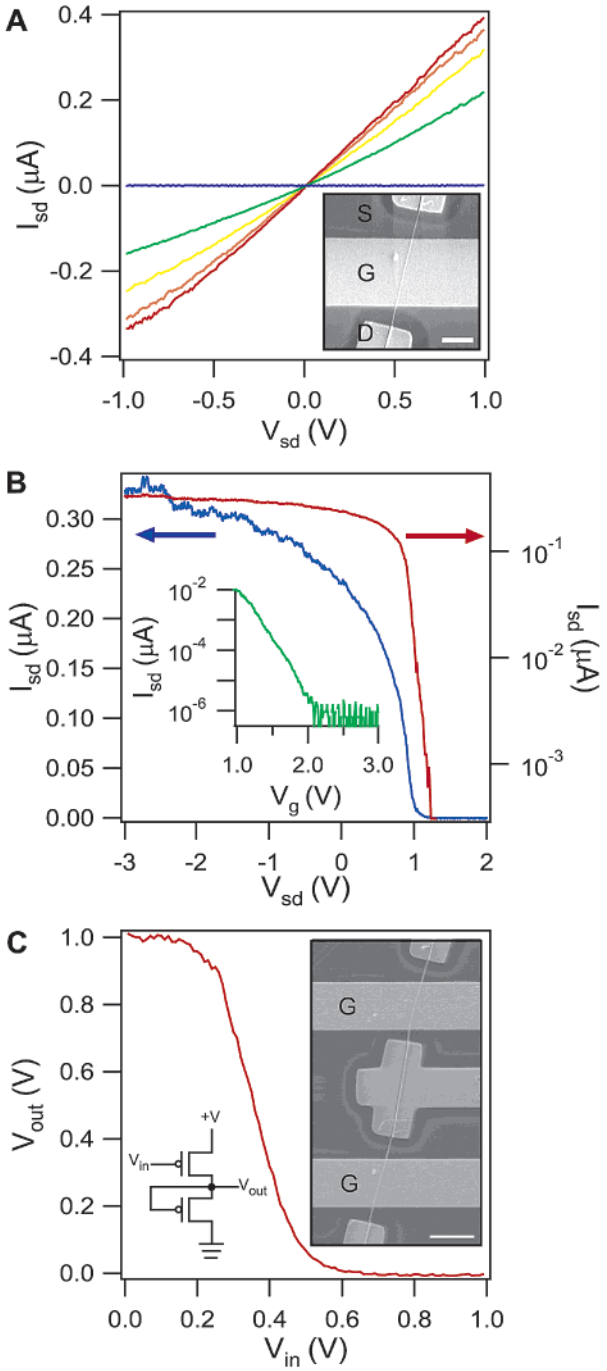

Figure 3. High-performance p-SiNW devices on plastic. (A) I_{sd} vs V_{sd} curves for a 20-nm SiNW transistor on a Mylar substrate, where the red, orange, yellow, green, and blue curves correspond to V_g = −3, −2, −1, 0, and 1 V, respectively. (Inset) SEM image of the NW device. The source (S), drain (D), and gate (G) are labeled. The scale bar is 1 μm. (B) I_{sd} vs V_g (V_{sd} = 1 V) for the device shown in A, plotted on a linear scale (left axis, blue curve) and log scale (right axis, red curve). (Inset) Data recorded at higher sensitivity. (C) V_{out} vs V_{in} for a NW inverter assembled from a p-SiNW on plastic. (Left inset) Schematic of the device. (Right inset) SEM image of the device, in which the NW is oriented in the vertical direction crossing two gates (G). The scale bar is 2 μm.

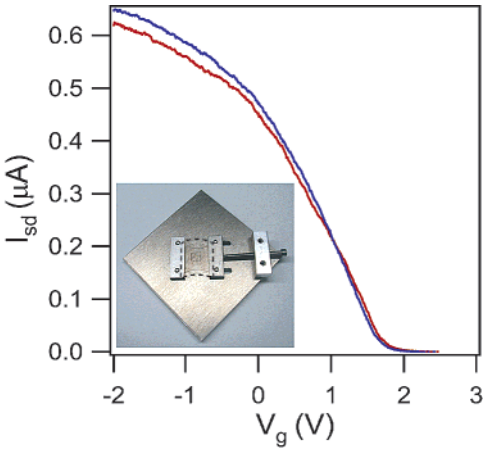

Figure 4. Effect of substrate bending on NW device performance. I_{sd} vs V_g for a NW transistor device measured when the substrate was flat (blue curve) and bent to a radius of curvature of 0.3 cm (red curve). (Inset) Photograph of the device used for bending the flexible plastic chip and securing it during measurement. The chip is highlighted with a black dashed line.

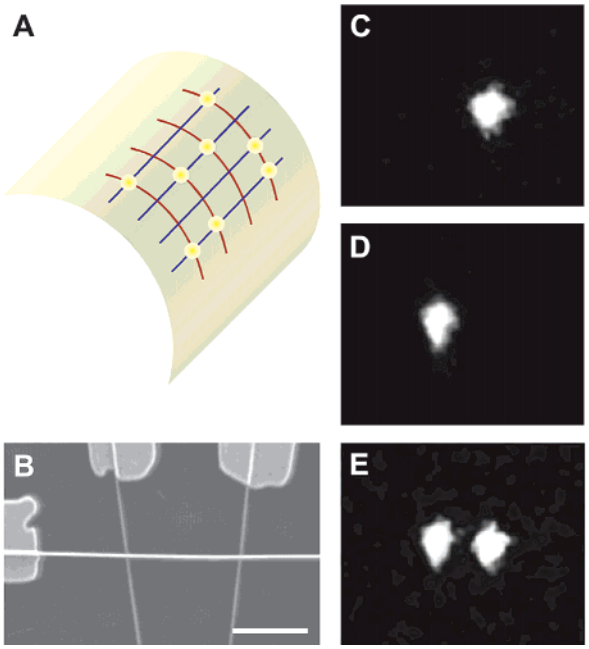

Figure 5. LED array on plastic. (A) Schematic of a flexible self-emitting display consisting of a crossed-NW LED array on a flexible plastic substrate. (B) SEM image of two p-SiNWs (vertical) crossing an n-type GaN NW to form two LEDs on the plastic substrate. The scale bar is 1 μm. (C−E) Electroluminescence (EL) images of localized emission from forward-biased Si−GaN junctions. The junctions can be driven individually (C, D) or simultaneously (E).

NW studies[36] suggest that similar values are possible. Last, the NW devices fabricated on plastic and glass could be readily improved without changing our fabrication strategy, for example, by using multi-NW devices to increase the on currents,[36] employing more sophisticated core/shell NW structures[18] designed to produce high mobilities, and/or by incorporating high-κ gate dielectrics.[37]

The assembly of high-performance SiNW devices on flexible plastic substrates can be readily extended to more complex structures. For example, we have configured a high aspect ratio p-SiNW as an inverter or logic NOT device (Figure 3c) by defining two FETs on a single NW. One of the transistors is used as a switch, and the other functions as a compensating resistor.[38] The voltage output (V_{out}) versus voltage input (V_{in}) of this device shows that V_{out} is high (1 V) when V_{in} is low (0 V) and that the output drops rapidly to a low value as the input is increased. This V_{out} versus V_{in} data shows that the inverter has a gain, $|dV_{out}/dV_{in}|$, of 4. The inverter operates within a 1-V range, which is significantly lower than the 5−10 V reported for inverters fabricated using organic transistors,[39,40] and thus has advantages for low-power applications.[38]

In addition, we have investigated the behavior of SiNW/plastic devices when bent because one of the potentially attractive features of plastic substrates is their flexibility. Significantly, a comparison of I_{sd} versus V_g data recorded when the NW/plastic device was flat versus bent to a radius of curvature of 0.3 cm (Figure 4) shows that there is only a small change in the bent state. There is a slight decrease in current for the device in the bent configuration, although this change is less than 10% for every point in the region of largest current drop, −2 to 1 V, with an average decrease of about 5%. This change is small given the large stress on the chip in the bent state and clearly shows the robust nature of our SiNW/plastic transistors and the potential for high-performance flexible devices.

Our approach for fabricating high-performance electronic devices on plastic and glass substrates is not limited to transistor devices and applications because the same strategy can be used to assemble NWs with different function. For example, the assembly of crossed-NW light-emitting diodes[17,20] (LEDs) on plastic substrates could enable the development of flexible self-emitting displays (Figure 5a) similar to organic LEDs.[41,42] Compared to organic LEDs, NWs have several advantages: (i) they are robust inorganic materials, (ii) different materials have a wide-range of spectrally pure output colors, and (iii) NW transistor drive and LED devices can be integrated together without the need for polycrystalline silicon. To investigate this concept, we assembled crossed-NW UV LEDs from n-type GaN NWs[16,17] and p-type SiNWs onto plastic substrates using sequential orthogonal fluid-directed assembly.[21] Significantly, when either one or both of the p−n diodes of a representative 1 × 2 n-GaN/p-Si crossed NW device (Figure 5b) were forward-biased, localized and addressable emission was observed from the junctions (Figure 5c−e). These NW UV LEDs can also maintain their emissive properties upon repeated cycles of bending/unbending of the plastic substrate and thus demonstrate the potential for the fabrication of high-performance optoelectronic systems on flexible plastics in the future.

We have shown that high-quality, single-crystal NWs can be assembled on glass and flexible plastic substrates to create FET and LED devices. In our approach, the high-temperature synthesis of single-crystal NWs has been separated from ambient-temperature solution-based assembly to enable the fabrication of single-crystal-like devices that greatly exceed the characteristics of amorphous silicon and organic materials, which have been widely investigated as materials for

developing lightweight and flexible electronic and display applications. In the future, it will be important to demonstrate NW assembly and reproducible device fabrication in a scalable manner. Recent studies employing scalable Langmuir−Blodgett and photolithography techniques, which have demonstrated control of the organization, hierarchical patterning, and interconnection of a large numbers of devices over large areas,[36,43] suggest that this latter challenge can be overcome. Last, it is worth noting that there remains substantial potential for high-density integration on these substrates because this approach should be scalable to ever increasing densities and smaller device sizes without any changes in the key building blocks.

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References

(1) Lueder, E. *Liquid Crystal Displays: Addressing Schemes and Electro-Optical Effects*; Wiley & Sons: Chichester, England, 2001.
(2) Service, R. F. *Science* **2000**, *287*, 415.
(3) Uchikoga, S. *MRS Bull.* **2002**, *27*, 881.
(4) Wisnieff, R. L.; Ritsko, J. J. *IBM J. Res. Dev.* **2000**, *44*, 409.
(5) Shaw, J. M.; Seidler, P. F. *IBM J. Res. Dev.* **2001**, *45*, 3.
(6) Chen, Y.; Au, J.; Kazlas, P.; Ritenour, A.; Gates, H.; McCreary, M. *Nature* **2003**, *423*, 136.
(7) Hara, A.; Takeuchi, F.; Takei, M.; Suga, K.; Yoshino, K.; Chida, M.; Sano, Y.; Sasaki, N. *Jpn. J. Appl. Phys., Part 2* **2002**, *41*, L311.
(8) Rogers, J. A.; Bao, Z.; Baldwin, K.; Dodabalapur, A.; Crone, B.; Raju, V. R.; Kuck, V.; Katz, H.; Amundson, K.; Ewing, J.; Drzaic, P. *Proc. Natl. Acad. Sci. U.S.A.* **2001**, *98*, 4835.
(9) Sirringhaus, H.; Kawase, T.; Friend, R. H.; Shimoda, T.; Inbasekaran, M.; Wu, W.; Woo, E. P. *Science* **2000**, *290*, 2123.
(10) Dimitrakopoulos, C. D.; Mascaro, D. J. *IBM J. Res. Dev.* **2001**, *45*, 11.
(11) Lieber, C. M. *MRS Bull.* **2003**, *28*, 486.
(12) Single-crystal p-SiNWs were grown via a gold-nanocluster-catalyzed method using 20-nm gold nanoclusters (Ted Pella) and SiH_4/B_2H_6 as the reactants.[14] A Si:B atomic ratio of 4000:1 was used for the NW transistors. The p-SiNW used to form p−n LEDs were core/shell structures[18] consisting of a 20-nm-diameter intrinsic silicon core and a 10-nm shell (250:1 Si:B). Single-crystal GaN NWs were prepared by nickel-metal-catalyzed chemical vapor deposition as described previously.[17] Stable solutions of NWs were prepared by sonication of the growth substrate in ethanol for 5−10 s.
(13) Cui, Y.; Zhong, Z.; Wang, D.; Wang, W. U.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 149.
(14) Cui, Y.; Duan, X.; Hu, J.; Lieber, C. M. *J. Phys. Chem. B* **2000**, *104*, 5213.
(15) Huang, Y.; Duan, X.; Cui, Y.; Lauhon, L. J.; Kim, K.-H.; Lieber, C. M. *Science* **2001**, *294*, 1313.
(16) Huang, Y.; Duan, X.; Cui, Y.; Lieber, C. M. *Nano Lett.* **2002**, *2*, 101.
(17) Zhong, Z.; Qian, F.; Wang, D.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 343.
(18) Lauhon, L. J.; Gudiksen, M. S.; Wang, D.; Lieber, C. M. *Nature* **2002**, *420*, 57.
(19) Duan, X.; Lieber, C. M. *Adv. Mater.* **2000**, *12*, 298.
(20) Duan, X.; Huang, Y.; Cui, Y.; Wang, J.; Lieber, C. M. *Nature* **2001**, *409*, 66.
(21) Huang, Y.; Duan, X.; Wei, Q.; Lieber, C. M. *Science* **2001**, *291*, 630.
(22) Devices were fabricated on alkali-free glass wafers (Plan Optik) and 100-μm-thick poly(ethylene terephthalate) (Mylar, CP Films) coated with ∼100-nm-thick indium tin oxide (ITO), which facilitates electron microscopy. The glass substrates were used without further treatment, and the plastic substrates were spin-coated with 500 nm of SU-8 (Microchem Corp.) and 50 nm of SiO_2 to isolate the conducting ITO and to provide a surface with good metal adhesion, respectively. Gate electrodes were defined either by photolithography or by electron beam lithography and were metallized via the thermal evaporation of Cr/Au (10 nm/40 nm). A 20-nm layer of SiO_2 was thermally deposited over the gate electrodes on the glass substrates to prevent shorting between the NWs and gates during annealing. Electrodes were defined by electron beam lithography and were metallized with Ni (80 nm), Pd (80 nm), and Ti/Au (60/60 nm) for glass, plastic, and plastic LED structures, respectively. No annealing was carried out on plastic substrates, although the contacts on glass were annealed at 250 °C (2 min) and 360 °C (1 min).
(23) Morales, A. M.; Lieber, C. M. *Science* **1998**, *279*, 208.
(24) Martel, R.; Schmidt, T.; Shea, H. R.; Hertel, T.; Avouris, Ph. *Appl. Phys. Lett.* **1998**, *73*, 2447.
(25) Sze, S. M. *Physics of Semiconductor Devices*; Wiley & Sons: New York, 1981.
(26) Stannowski, B.; Schropp, R. E. I.; Wehrspohn, R. B.; Powell, M. J. *J. Non-Cryst. Solids* **2002**, *299−302*, 1340.
(27) Wong, W. S.; Ready, S.; Matusiak, R.; White, S. D.; Lu, J.-P.; Ho, J.; Street, R. A. *J. Non-Cryst. Solids* **2002**, *299−302*, 1335.
(28) Gleskova, H.; Wagner, S.; Gasparik, V.; Kovac, P. *J. Electrochem. Soc.* **2001**, *148*, G370.
(29) Hsu, P. I.; Bhattacharya, R.; Gleskova, H.; Huang, M.; Xi, Z.; Suo, Z.; Wagner, S.; Sturm, J. C. *Appl. Phys. Lett.* **2002**, *81*, 1723.
(30) Halik, M.; Klauk, H.; Zschieschang, U.; Schmid, G.; Radlik, W.; Weber, W. *Adv. Mater.* **2002**, *14*, 1717.
(31) Klauk, H.; Halik, M.; Zschieschang, U.; Eder, F.; Schmid, G.; Dehm, C. *Appl. Phys. Lett.* **2003**, *82*, 4175.
(32) Kim, Y.-M.; Pyo, S.-W.; Kim, J.-S.; Shim, J.-H.; Suh, C.-H.; Kim, Y.-K. *Opt. Mater.* **2002**, *21*, 425.
(33) Knipp, D.; Street, R. A.; Völkel, A.; Ho, J. *J. Appl. Phys.* **2003**, *93*, 347.
(34) Gosain, D. P. *Proc. SPIE* **2002**, *4426*, 394.
(35) Shimoda, T.; Inoue, S.; Utsunomiya, S. *Proc. SPIE* **2001**, *4295*, 52.
(36) Jin, S.; Whang, D.; Wu, Y.; McAlpine, M. C.; Friedman, R. S.; Lieber, C. M. Unpublished results.
(37) Javey, A.; Kim. H.; Brink, M.; Wang, Q.; Ural, A.; Guo, J.; McIntyre, P.; McEuen, P.; Lundstrom, M.; Dai, H. *Nat. Mater.* **2002**, *1*, 241.
(38) Horowitz, P.; Hill, W. *The Art of Electronics*; Cambridge University Press: Cambridge, England, 1989.
(39) Rogers, J. A.; Dodabalapur, A.; Bao, Z.; Katz, H. E. *Appl. Phys. Lett.* **1999**, *75*, 1010.
(40) Gelinck, G. H.; Geuns, T. C. T.; de Leeuw, D. M. *Appl. Phys. Lett.* **2000**, *77*, 1487.
(41) Sheats, J. R. Antoniadis, H.; Hueschen, M.; Leonard, W.; Miller, J.; Moon, R.; Roitman, D.; Stocking, A. *Science* **1996**, *273*, 884.
(42) Howard, W. E.; Prache, O. F. *IBM J. Res. Dev.* **2001**, *45*, 115.
(43) Whang, D.; Jin, S.; Wu, Y.; Lieber, C. M. *Nano Lett.* **2003**, *3*, 1255.

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