

Bridging Length Scales in 2D Semiconductor Manufacturing through Programmable Chemistry and Interfaces

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A central challenge in the manufacturing of two-dimensional (2D) semiconductors lies not in achieving atomic-scale precision, high-quality crystal growth or wafer-scale integration individually, but in **preserving materials control across the disparate length scales that connect them**. Although substantial advances have been made in precursor chemistry, crystal synthesis, transfer processes and device fabrication, these achievements often remain disconnected. Such discontinuities represent a fundamental manufacturing gap: the structural and electronic quality established during materials synthesis is not necessarily preserved through subsequent processing and integration. Bridging these gaps requires strategies that translate atomic-scale chemical control into predictable crystal assembly, process-compatible interfaces and ultimately wafer-scale electronic functionality.

In this talk, I will present two complementary approaches to closing these manufacturing gaps through the rational engineering of chemical reaction pathways and growth interfaces. The first establishes a hierarchical manufacturing strategy that connects **ångström-scale precursor chemistry to wafer-scale single-crystalline WS₂**. Stoichiometric precursor engineering directs thermodynamically favored reaction pathways towards the spontaneous formation of a geometrically confined interfacial buffer. By homogenizing the adsorption-energy landscape and suppressing heterogeneous nucleation, this buried interface translates molecular-level chemical design into controlled micrometer-scale crystal assembly and ultimately wafer-scale, crystallographically aligned monolayer films. Crucially, the same interfacial buffer also serves as a growth-defined release layer, enabling direct delamination of WS₂ from sapphire in deionized water without polymer supports or corrosive etchants. The released monolayers retain an ultralow surface roughness of approximately 0.2 nm and exhibit an average field-effect mobility of 100 cm² V⁻¹ s⁻¹, a subthreshold swing of 85 mV dec⁻¹ and threshold-voltage hysteresis of only 37 mV. The strategy is further applicable to bilayer WS₂ and monolayer MoS₂ and WSe₂, demonstrating its versatility across representative transition-metal dichalcogenides. These findings establish a form of **transfer-ready epitaxy in which crystal growth and subsequent integration are engineered through a common interfacial design principle**.

The second approach addresses a complementary manufacturing challenge: the direct synthesis of high-performance p-type 2D semiconductors on amorphous dielectrics, eliminating the need for post-growth transfer. By engineering the metal-vapor-catalyzed dissociation pathways and nucleation energetics of monomethylamine borane (MMAB), we achieve continuous crystalline boron carbon nitride (BCN) films without requiring epitaxial registry with the underlying substrate. Carbon substitution at nitrogen sites introduces p-type transport, expanding the available materials palette for complementary 2D electronics. Wafer-scale arrays of top-gated BCN transistors exhibit a field-effect hole mobility of 80 cm² V⁻¹ s⁻¹, on-currents exceeding 500 μA μm⁻¹, an on/off current ratio of 10⁹, an interface-trap density of 5 × 10¹¹ cm⁻² and a threshold voltage of -0.45 V. This direct-growth strategy circumvents the constraints associated with crystalline growth substrates and transfer-induced interface degradation, providing a promising route towards dielectric-compatible p-type electronics.

Together, these studies establish two complementary pathways—transfer-ready epitaxy and transfer-free dielectric growth—for bridging the manufacturing discontinuities between materials synthesis and device integration. By encoding control over crystal nucleation, interfacial structure and processing compatibility at the precursor level, these approaches provide a foundation for translating atomic-scale materials design into wafer-scale manufacturing, with implications for monolithic three-dimensional integration of complementary semiconductor technologies.

Reference:

[1] *Nature* 658, 389 (2026) [2] *Nature* (2026), Accepted [3] *Nature Photonics* 20, 765 (2026) [4] *Nature Electronics* 8, 1136 (2026) [5] *Nature Materials* 25, 1293 (2026) [6] *Nature Nanotechnology* 18, 1289 (2023)



Biography

Vincent Tung completed his Ph.D. at the University of California, Los Angeles (UCLA) and was an Institute for Sustainability and Energy at Northwestern (ISEN) postdoctoral fellow at Northwestern University. He has been a Professor at the Department of Chemical System Engineering at the University of Tokyo since July 2022. He is the recipient of the NSF CAREER Award, New Doctoral Investigator of ACS Petroleum Award, Research Excellence of the University of California System, and Young Scientist Award for eMRS. His research interests are in materials chemistry, processing, and epitaxy-grown two-dimensional (2D) layered materials and their vdW heterostructures for next-generation semiconductors.