State-of-the-art device fabrication techniques

- Standard Photo-lithography and e-beam lithography
- Advanced lithography techniques used in semiconductor industry
Lithographic process:

**Deposition:** Thermal evaporation, e-gun deposition, DC & RF sputtering, Chemical vapor deposition (LPCVD, PECVD, APCVD) Electrochemical deposition

**Patterning techniques:**

- **Etching**
  - Wet-etching
  - Dry-etching
  - Reactive ion etching, RIE
  - Inductively coupled plasma etcher, ICP
  - Electro-cyclotron resonance etcher, ECR
  - TCP, SWP, …

- **Lift-off**
Standard etching process

1. CVD, Thermal, e-gun, Sputtering, spin-coating

2. Spin-coating

3. Photoresist

4. UV light (contact, projection)

5. Mask plate

6. Coated film

7. Develop (remove exposed part for positive-tone PR)

8. Selective dry/wet etching

9. Remove resist mask

10. Finished pattern
Complementary process: lift-off

1. **Spin-coating**
   - photoresist

2. **Contact, projection**
   - mask plate

3. **UV light**
   - expose photoresist

4. **Develop**
   - remove exposed part (for positive-tone PR)
   - Thermal, e-gun, Sputtering

5. **Lift-off**
   - remove resist mask excess film

6. **Finished pattern**
Substrate treatment process

1. Spin-coating
2. Contact or Projection exposure
3. Selective dry/wet etching or doping
4. Remove resist mask
5. Finished pattern
Mix and Match technology

Photolithography

E-beam lithography

align key

align key

7 mm

80 µm
Moore’s Law:

a 30% decrease in the size of printed dimensions every two years

“Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate.”

Transistor dimensions scale to improve performance, reduce power and reduce cost per transistor.
SOURCES OF RADIATION FOR MICROLITHOGRAPHY

Minimum feature size is scaling faster than lithography wavelength
Advanced photo mask techniques help to bridge the gap
The Ultimates of Optical Lithography

Resolution: \( R = k_1 \left( \frac{\lambda}{NA} \right) \)

\( \text{NA} = \sin \theta = \text{numerical aperture} \)

\( K_1 = \text{a constant for a specific lithography process} \)

smaller \( K_1 \) can be achieved by

improving the process or resist contrast

Depth of Focus \( \text{DoF} = k_2 \left( \frac{\lambda}{NA^2} \right) \)

Calculated \( R \) and \( \text{DoF} \) values

<table>
<thead>
<tr>
<th>UV wavelength</th>
<th>248 nm</th>
<th>193 nm</th>
<th>157 nm</th>
<th>13.4 nm</th>
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<tbody>
<tr>
<td>Typical NA</td>
<td>0.75</td>
<td>0.75</td>
<td>0.75</td>
<td>0.25</td>
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<tr>
<td>Production value of ( k_1 )</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
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<tr>
<td>Resolution</td>
<td>0.17 ( \mu \text{m} )</td>
<td>0.13 ( \mu \text{m} )</td>
<td>0.11 ( \mu \text{m} )</td>
<td>0.027 ( \mu \text{m} )</td>
</tr>
<tr>
<td>DoF (assuming ( k_2 = 1 ))</td>
<td>0.44 ( \mu \text{m} )</td>
<td>0.34 ( \mu \text{m} )</td>
<td>0.28 ( \mu \text{m} )</td>
<td>0.21 ( \mu \text{m} )</td>
</tr>
</tbody>
</table>

P.F. Carcia et al. DuPoint Photomasks, Vacuum and Thin Film (1999)
Optical Proximity Correction

used in 90 nm (193nm) production line

Mark Bohr, Intel 2003
Two types of phase shift mask

Alternating aperture phase shift mask

1. dark line appears at the center
2. Applicable only in limited structures

Embedded attenuating phase shift mask

1. Can even improve DoF
2. Use MoSi$_x$O$_y$N$_z$, SiN$_x$ or CrO$_x$F$_y$ instead of Cr

Ref: P.F. Carcia et al. DuPoint Photomasks, Vacuum and Thin Film (1999)
Immersion lithography

- A photolithography resolution enhancement technique
- A liquid medium fills the gap between the final lens and the wafer surface
- The liquid medium has a refractive index greater than one.
- The resolution is increased by a factor equal to the refractive index of the liquid.
- Current immersion lithography tools use highly purified water for this liquid, achieving feature sizes below 45 nanometers

- Currently, the most promising high-index lens material is lutetium aluminum garnet, with a refractive index of 2.14.
- High-index immersion fluids are approaching refractive index values of 1.7.
- These new developments allow the optical resolution to approach ~30 nm.

- Double patterning has received interest recently since it can potentially increase the half-pitch resolution by a factor of 2.
- This could allow the use of immersion lithography tools beyond the 32 nm node, potentially to the 16 nm node.
**Double patterning**

For the semiconductor industry, double patterning is the only lithography technique to be used for the 32 nm and 22 nm half-pitch nodes in 2008–2009 and 2011–2012, respectively, using tools already available today.

**Single Exposure**

**Dual-tone photoresist**

The lowest and highest doses of a single exposure result in insolubility, while the intermediate doses allow the photoresist to be removed by developer.

**Dual-Tone Development**

Two develop steps remove highest and lowest exposure dose regions of the photoresist, leaving the intermediate dose edges.

State-of-the-art 193 nm tool with a numerical aperture of 1.35 can extend its resolution to 18 nm half-pitch with double patterning. Due to this ability to use coarse patterns to define finer patterns, it offers an immediate opportunity to achieve resolution below 30 nm without the need to address the technical challenges of expensive next-generation lithography technologies such as EUV.

Even electron beam lithography may eventually require double patterning (due to secondary electron scattering) to achieve comparable half-pitch resolution, for instance, in the fabrication of 15 nm half-pitch X-ray zone plates.
EUV reflective mask

EUV exposure

These electrons increase the extent of chemical reactions in the resist, beyond that defined by the original light intensity pattern. As a result, a secondary electron pattern that is random in nature is superimposed on the optical image. The unwanted secondary electron exposure results in loss of resolution, observable line edge roughness and linewidth variation.

EUV radiation (red) reflected from the mask pattern is absorbed in the resist (amber) and substrate (brown), producing photoelectrons and secondary electrons (blue).

Intel EUV mask

EUV multilayer and absorber (purple) constituting mask pattern for imaging a line.
EUV exposure tool

- Uses very short 13.4 nm light
- 13.4 nm radiation absorbed by all materials
- Requires reflective optics coated with quarter-wave Bragg reflectors
- Uses reflective reticles with patterned absorbers
- Vacuum operation
- Unique source for EUV light

NXE:3100

22 February 2010: TSMC to purchase EUV lithography system from ASML
Electron Beam Lithography:

楊富量 (NDL), Outlook for 15nm CMOS Manufacture
Projection EBL Systems (SCALPEL): 

scattering with angular limitation in projection electron beam lithography

beam of electrons

membrane scatterer

screening mask

Lens 1

back focal plane filter

reduced image on Lens 2
Multibeam direct-write electron beam lithography system

Single source with correction lens array

~50 wafers/hr

Multi-source with single electron optical column

~60 wafers/hr

Canon Inc.,

Ion Diagnostics Incorporated

[Diagram of multibeam direct-write electron beam lithography system]
More than 10,000 parallel electron beams.

Fibre-optics is capable of transporting a large quantity of information.

In October 2008, Mapper and Taiwan Semiconductor Manufacturing Co. have signed an agreement, according to which Mapper will ship its first 300mm multiple-electron-beam maskless lithography platform for process development and device prototyping to TSMC.
Material Engineering gains importance!
90 nm Generation Transistor

This is nano technology!
Experimental transistors for future process generations

- **65nm process**
  - 2005 production

- **45nm process**
  - 2007 production
  - CMOS
  - 0.8 nm conventional gate oxide

- **32nm process**
  - 2009 production

- **22nm process**
  - 2011 production

Intel C. Michael Garner Sept. 2003 NanoSIG
Nano materials will play an important role in the silicon nanotechnology platform

Interconnectors with high electrical conductivity

Low K interlevel Dielectric

High K gate oxide

Strained Si

Photoresist

## Introduction of new materials

<table>
<thead>
<tr>
<th></th>
<th>1997</th>
<th>1999</th>
<th>2001</th>
<th>2003</th>
<th>2005</th>
<th>2007</th>
<th>2009</th>
<th>2011</th>
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<tr>
<td><strong>1st Production</strong></td>
<td>1997</td>
<td>1999</td>
<td>2001</td>
<td>2003</td>
<td>2005</td>
<td>2007</td>
<td>2009</td>
<td>2011</td>
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<tr>
<td><strong>Process Generation</strong></td>
<td>0.25µm</td>
<td>0.18µm</td>
<td>0.13µm</td>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
<td>32 nm</td>
<td>22 nm</td>
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<tr>
<td><strong>Wafer Size (mm)</strong></td>
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<td>200</td>
<td>200/300</td>
<td>300</td>
<td>300</td>
<td>300</td>
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<tr>
<td><strong>Inter-connect</strong></td>
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<td>Al</td>
<td>Al</td>
<td>Cu</td>
<td>Cu</td>
<td>Cu</td>
<td>Cu</td>
<td>?</td>
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<tr>
<td><strong>Channel</strong></td>
<td>Si</td>
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<td>Si</td>
<td>Strained Si</td>
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<tr>
<td><strong>Gate dielectric</strong></td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>High-k</td>
<td>High-k</td>
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</tr>
<tr>
<td><strong>Gate electrode</strong></td>
<td>PolySi</td>
<td>PolySi</td>
<td>PolySi</td>
<td>PolySi</td>
<td>PolySi</td>
<td>Metal</td>
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source: Intel develop forum
Introduction of high-K gate dielectric

90 nm process

<table>
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<tr>
<th>Capacitance</th>
<th>1X</th>
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<tr>
<td>Leakage</td>
<td>1X</td>
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Experimental high-K

<table>
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<tr>
<th>Capacitance</th>
<th>1.6X</th>
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<tr>
<td>Leakage</td>
<td>&lt;0.01X</td>
</tr>
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</table>

Carolyn Block, Intel 2003
A message from Intel

Compress P-doped regions
by filling SiGe into carved trenches, hole conduction increased by 25%

Stretch N-doped regions
by annealing SixNy cover layer, electron conduction increased by 10%

Strained silicon benefits
• Strained silicon lattice increases electron and hole mobility
• Greater mobility results in 10-20% increase in transistor drive current (higher performance)
• Both NMOS and PMOS transistors improved
Three types of new Fully Depleted Transistors

- SOI wafer
  - Si
  - BOX

Handling Si wafer

Planar fully depleted SOI

Non-planar Double-gate (FinFET)

Non-planar Tri-gate
Fully Depleted Transistors made on SOI wafers

Non-planar Double-gate (FinFET)

Non-planar Tri-gate

Raised S-D using Selective Epi-Si Deposition

Robert Chau, Intel, 61st Device Research Conference June 2003
From Tri-gate transistors to Nano-wire transistors

deployment electric field

Tri-gate transistor

Nano-wire transistor