State-of-the-art device fabrication techniques

♣ **Standard Photo-lithography and e-beam lithography**

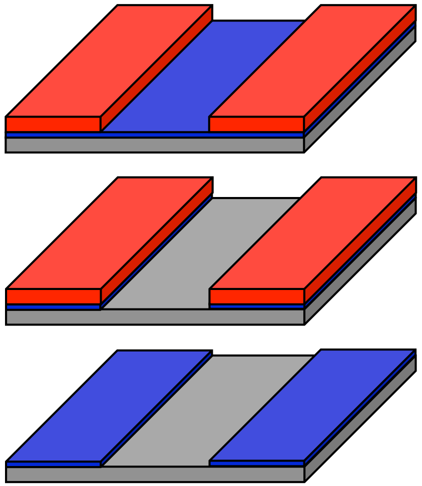
♣ **Advanced lithography techniques used in semiconductor industry**

Lithographic process:

Deposition: Thermal evaporation, e-gun deposition, DC & RF sputtering,
Chemical vapor deposition (LPCVD, PECVD, APCVD)
Electrochemical deposition

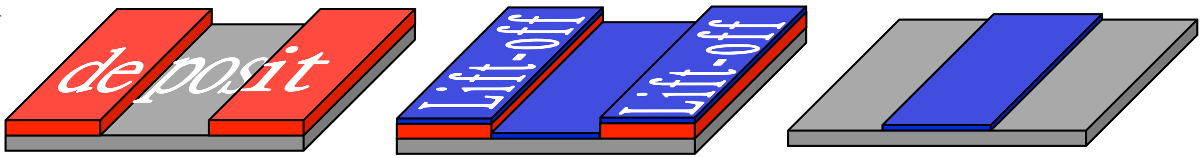
Patterning techniques:

Etching

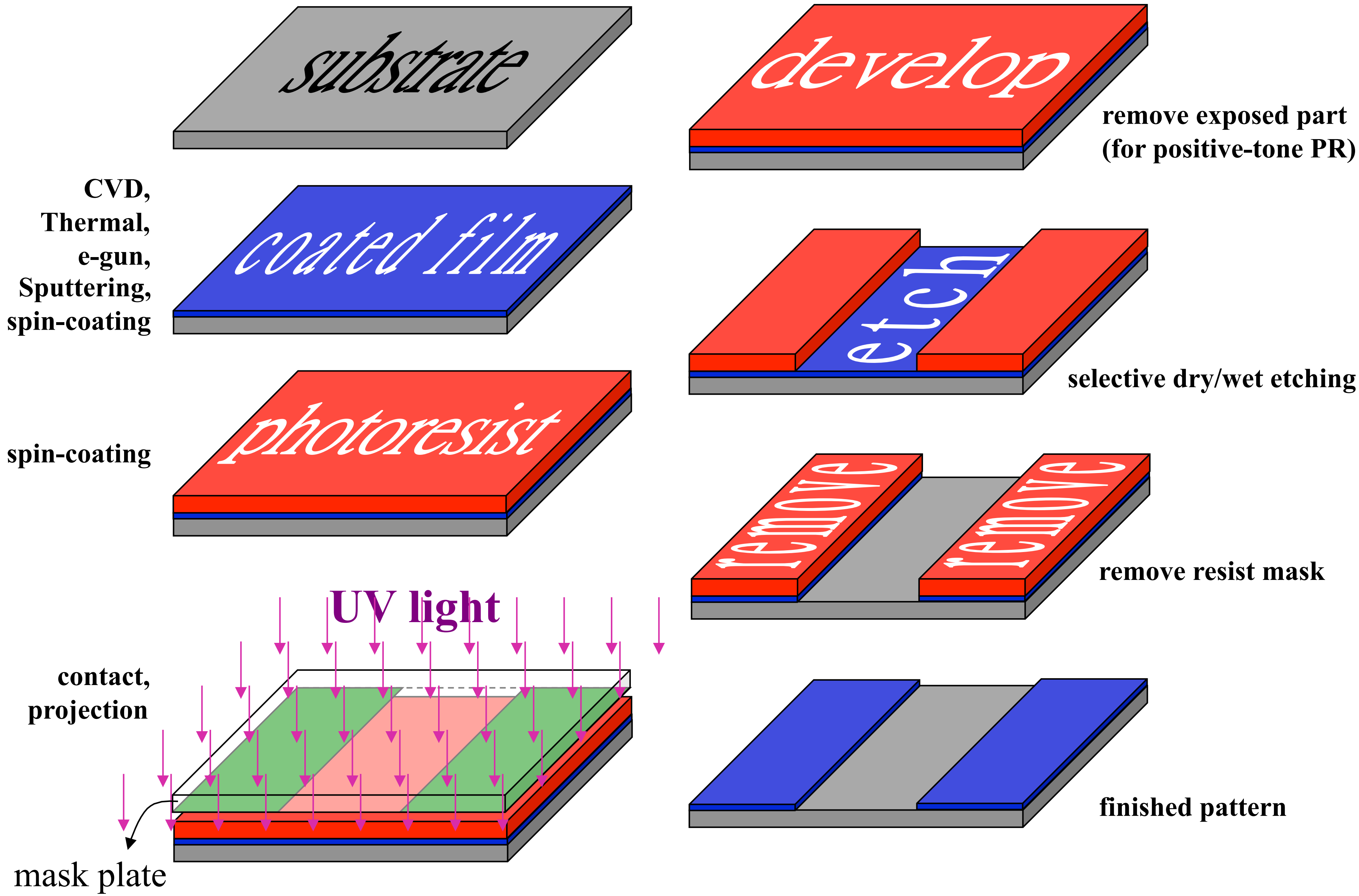


- **Wet-etching**
  - isotropic
  - anisotropic √
- **Dry-etching**
  - Reactive ion etching, RIE √
  - Inductively coupled plasma etcher, ICP √
  - Electro-cyclotron resonance etcher, ECR
  - TCP, SWP, …

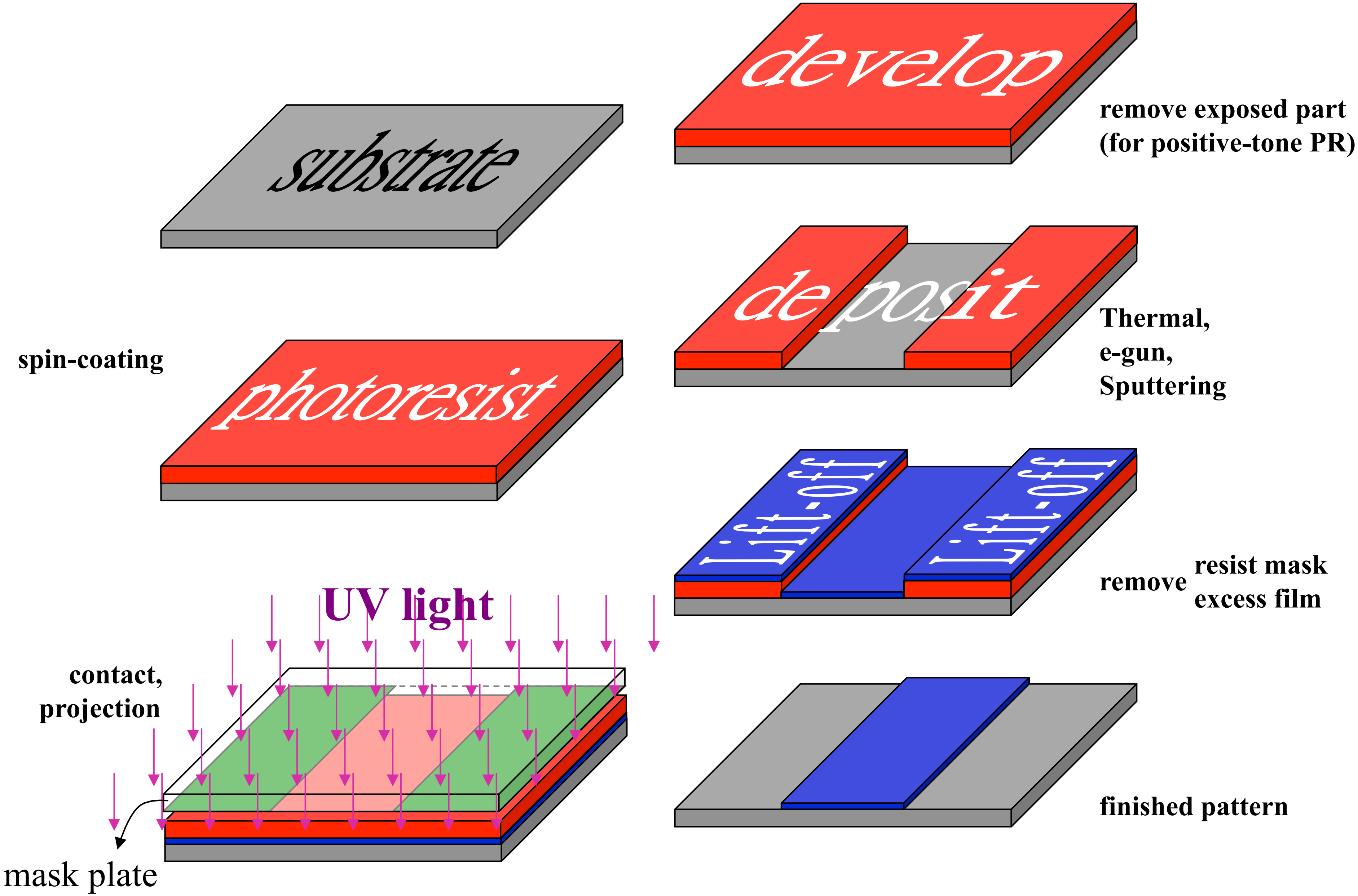
Lift-off √



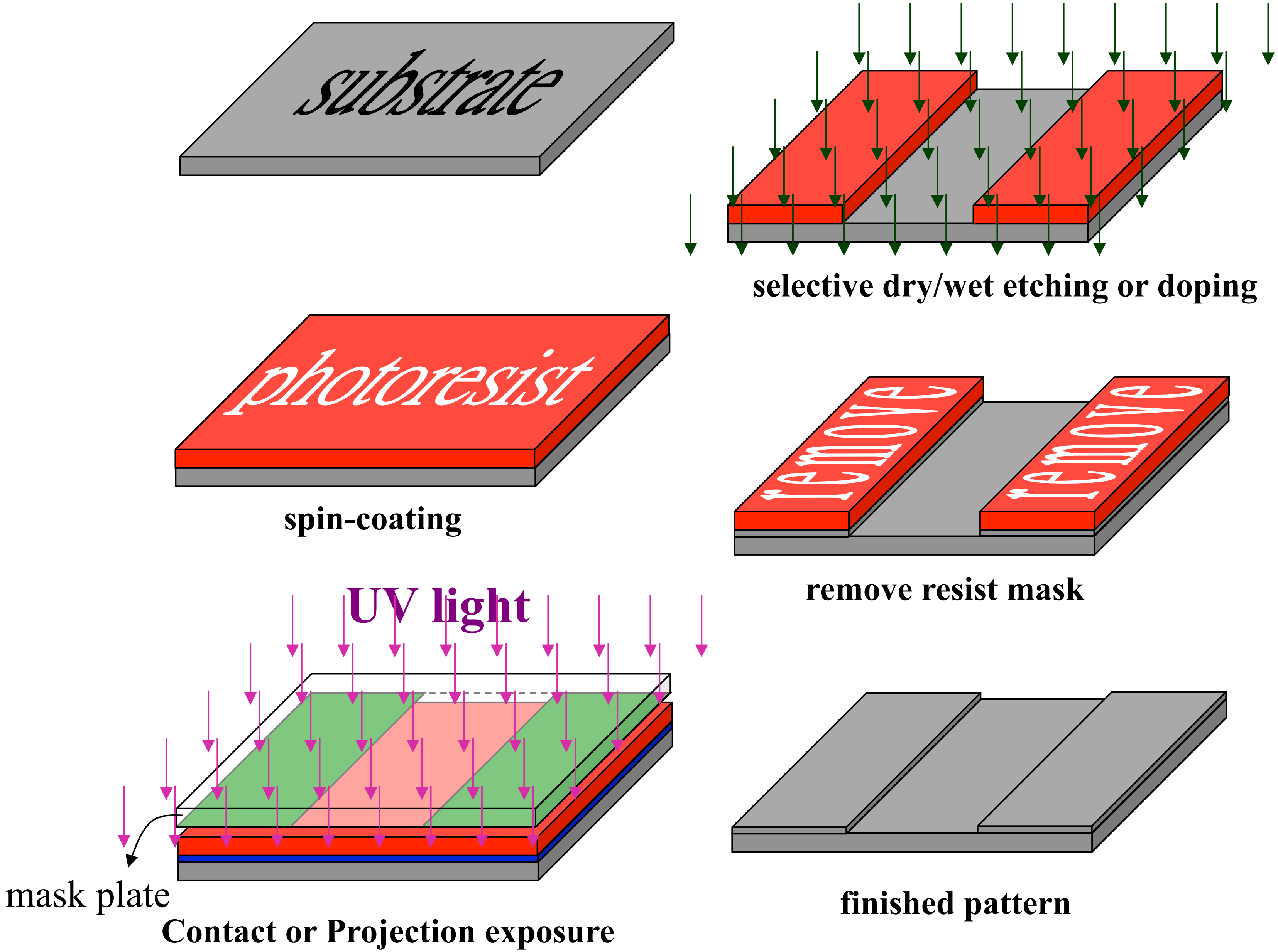
Standard etching process



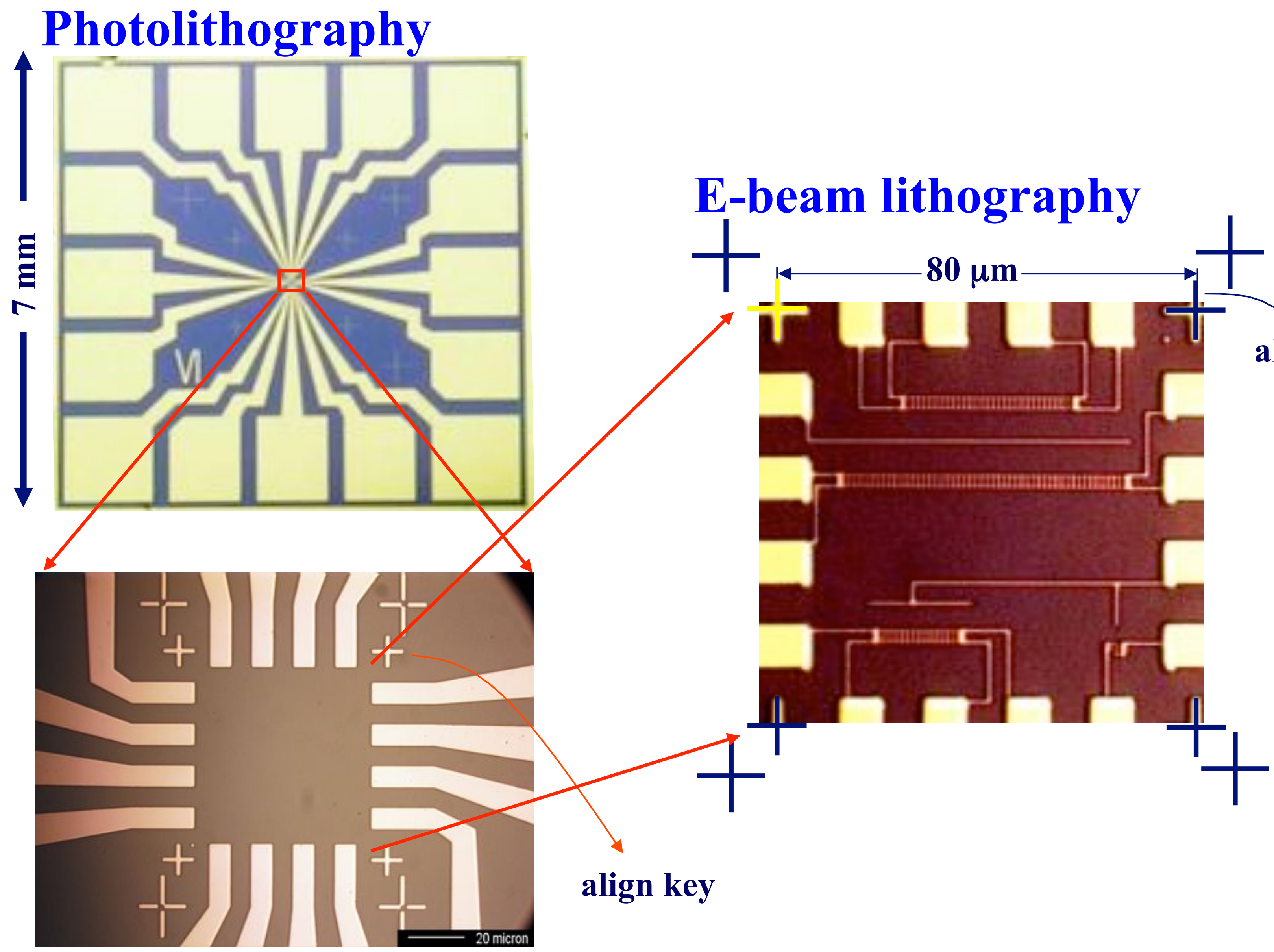
Complementary process: lift-off



Substrate treatment process

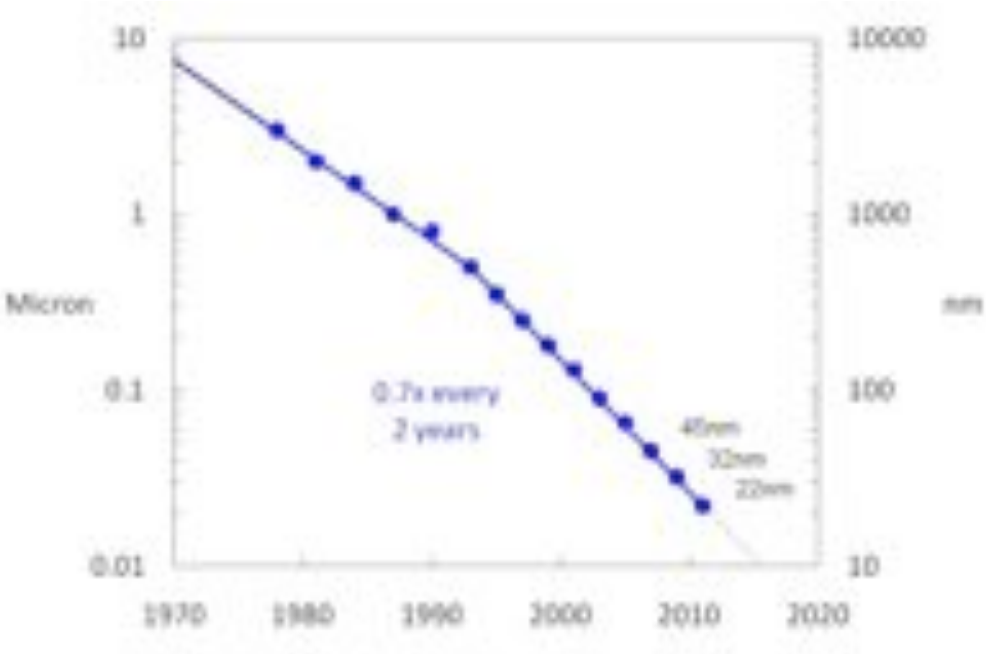


Mix and Match technology



Moore's Law:

a 30% decrease in the size of printed dimensions every two years



tens of billions of instructions per second

"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."

Transistor dimensions scale to improve performance, reduce power and reduce cost per transistor.

SOURCES OF RADIATION FOR MICROLITHOGRAPHY

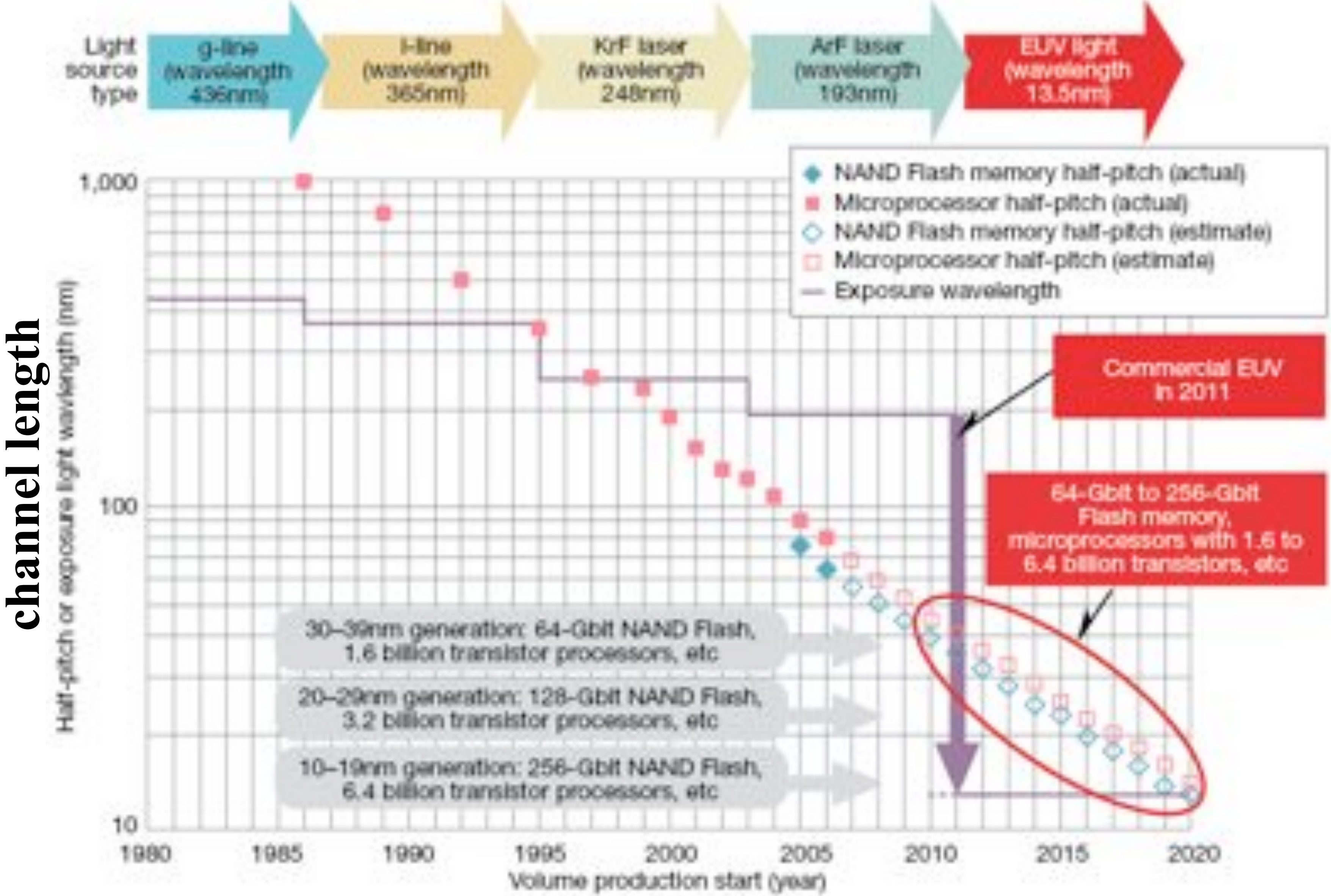
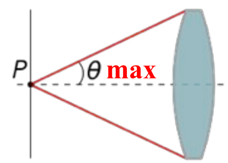


Diagram by Nikkei Electronics based on materials from Intel, International Technology Roadmap for Semiconductors (ITRS), etc.
http://www.newmaker.com/news_41958.html

Minimum feature size is scaling faster than lithography wavelength

Advanced photo mask techniques help to bridge the gap

The Ultimates of Optical Lithography



Resolution: $R=k_1 (\lambda/NA)$

NA = sinθ = numerical aperture

K_1 = a constant for a specific lithography process

smaller K1 can be achieved by improving the process or resist contrast

Depth of Focus $DoF=k_2 (\lambda/NA^2)$

Calculated R and DoF values

UV wavelength	248 nm	193 nm	~~157 nm~~	13.4 nm
Typical NA	0.75	0.75	~~0.75~~	0.25
Production value of k_1	0.5	0.5	~~0.5~~	0.5
Resolution	0.17 μm	0.13 μm	~~0.11 μm~~	0.027 μm
DoF (assuming k_2 = 1)	0.44 μm	0.34 nm	~~0.28 μm~~	0.21 μm

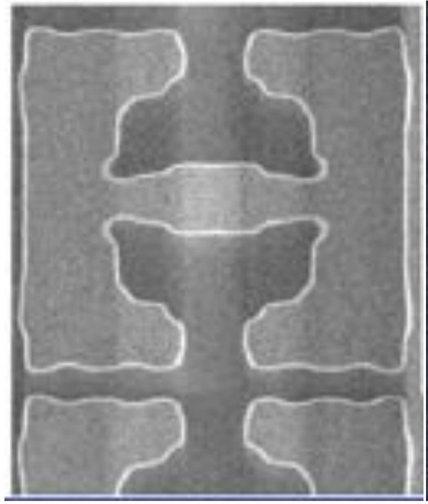
P.F. Carcia et al. DuPoint Photomasks, Vacuum and Thin Film (1999)

Optical Proximity Correction

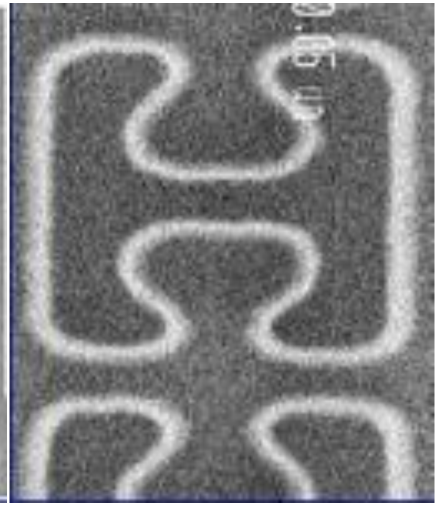
used in 90 nm (193nm) production line

Drawn structure

Add OPC features



Mask structure



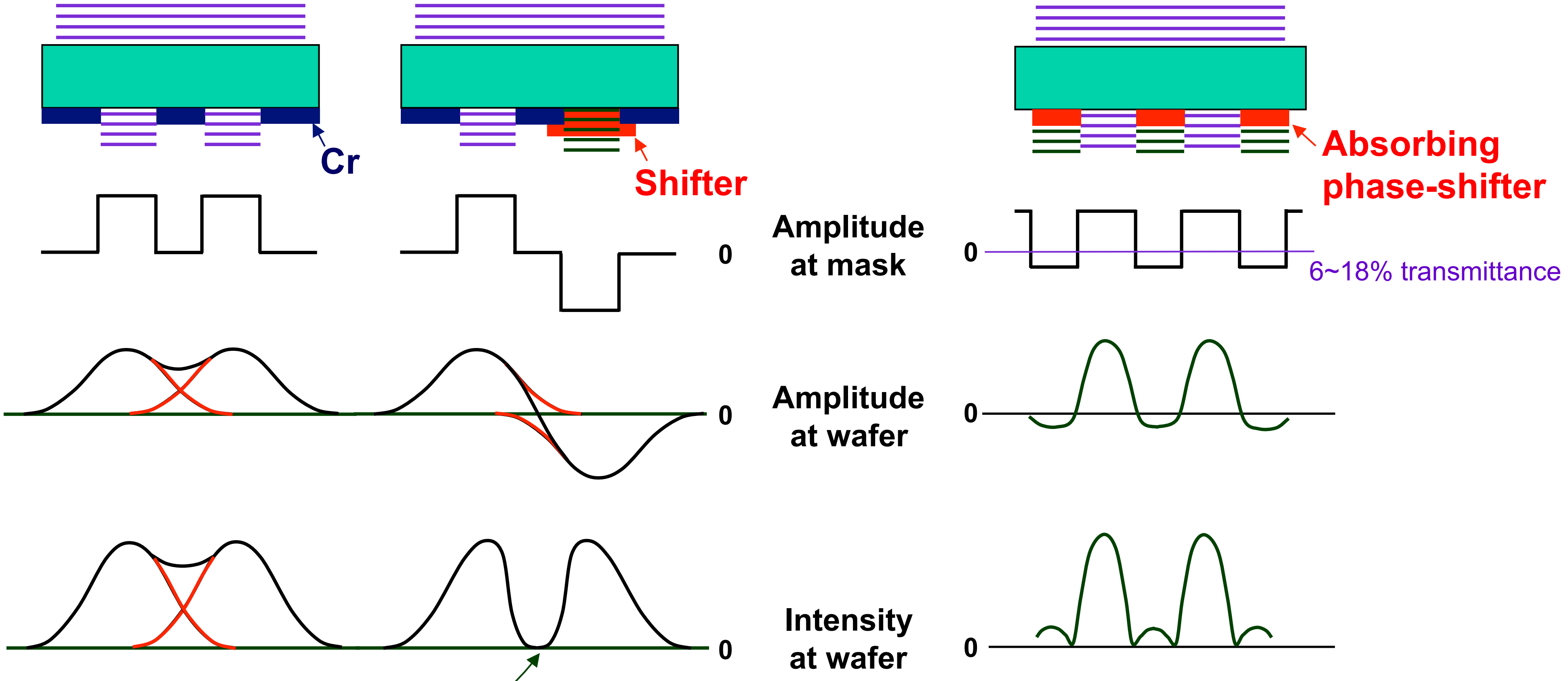
Printed on wafer

Mark Bohr, Intel 2003

Two types of phase shift mask

Alternating aperture phase shift mask

Embedded attenuating phase shift mask

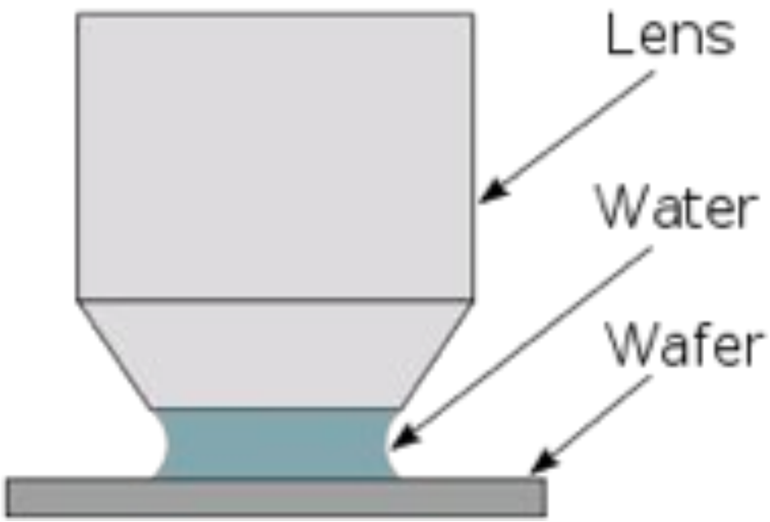


1. dark line appears at the center
2. Applicable only in limited structures

1. Can even improve DoF
2. Use $MoSi_xO_yN_z$, SiN_x or CrO_xF_y instead of Cr

Ref: P.F. Carcia et al. DuPoint Photomasks, Vacuum and Thin Film (1999)

Immersion lithography



✔a photolithography resolution enhancement technique
✔a liquid medium fills the gap between the final lens and the wafer surface
✔ the liquid medium has a refractive index greater than one.
✔ The resolution is increased by a factor equal to the refractive index of the liquid.
✔ Current immersion lithography tools use highly purified water for this liquid, achieving feature sizes below 45 nanometers

✔ Currently, the most promising high-index lens material is lutetium aluminum garnet, with a refractive index of 2.14.
✔ High-index immersion fluids are approaching refractive index values of 1.7.
✔ These new developments allow the optical resolution to approach ~30 nm.

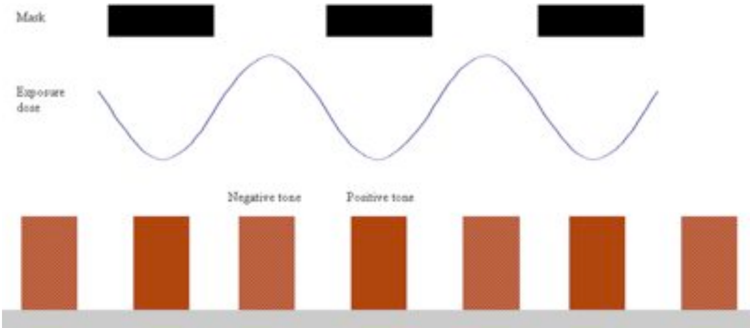
✖ Double patterning has received interest recently since it can potentially increase the half-pitch resolution by a factor of 2.
✖ This could allow the use of immersion lithography tools beyond the 32 nm node, potentially to the 16 nm node.

Double patterning

For the semiconductor industry, double patterning is the only lithography technique to be used for the 32 nm and 22 nm half-pitch nodes in 2008-2009 and 2011–2012, respectively, using tools already available today.

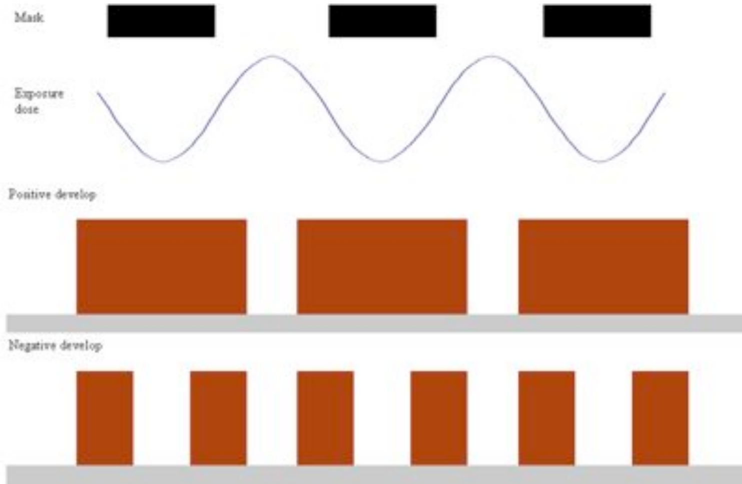
Single Exposure

Dual-tone photoresist



The lowest and highest doses of a single exposure result in insolubility, while the intermediate doses allow the photoresist to be removed by developer.

Dual-Tone Development



Two develop steps remove highest and lowest exposure dose regions of the photoresist, leaving the intermediate dose edges.

http://en.wikipedia.org/wiki/Double_patterning

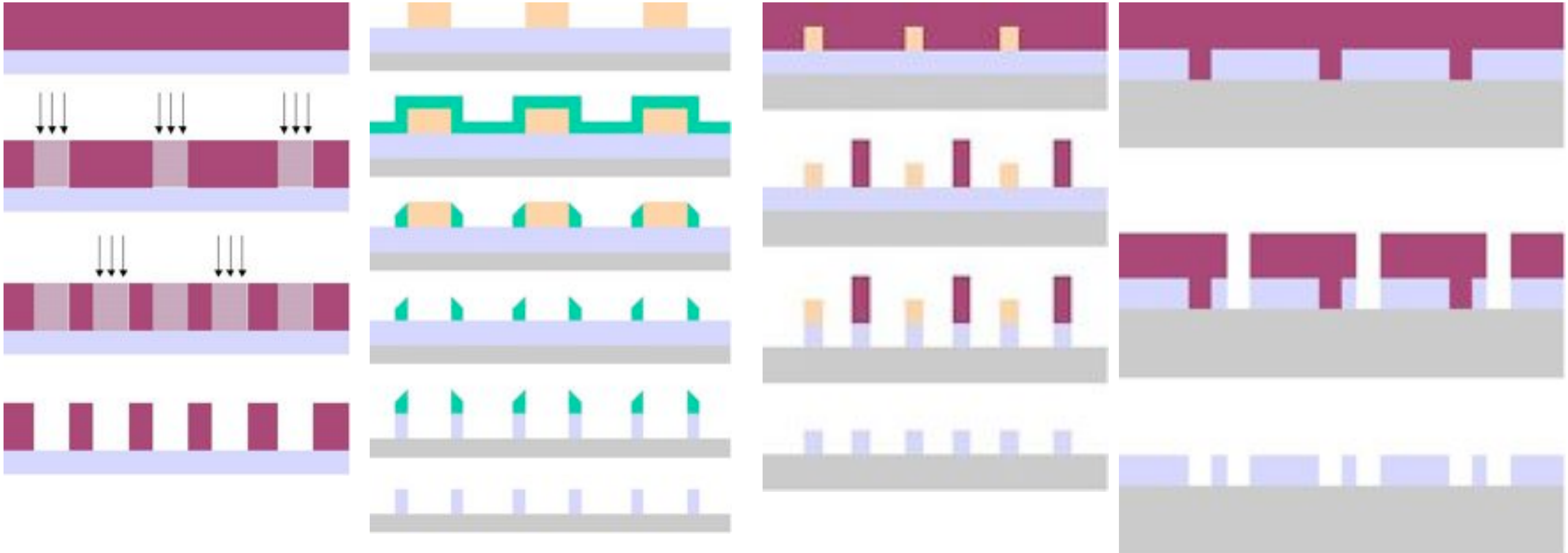
Double Patterning

Double exposure:
photoresist coating;
first exposure;
second exposure;
development

Self-aligned spacer:
first pattern;
deposition;
spacer formation by etching;
first pattern removal;
etching with spacer mask;
final pattern

Double Expose, Double Etch (lines):
Photoresist coating over first pattern;
photoresist features between previous features;
etching;
mask removal

Double Expose, Double Etch (trenches):
Photoresist coating over first pattern;
etching adjacent to previous features;
mask removal



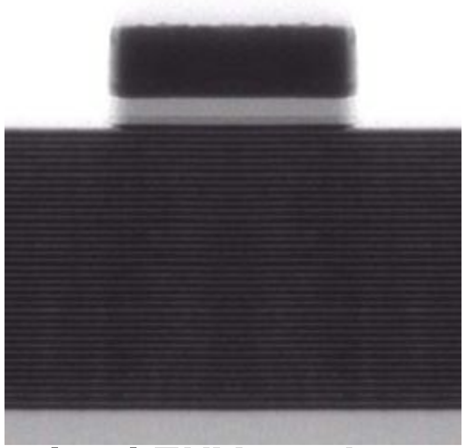
State-of-the-art 193 nm tool with a numerical aperture of 1.35 can extend its resolution to 18 nm half-pitch with double patterning.

Due to this ability to use coarse patterns to define finer patterns, it offers an immediate opportunity to achieve resolution below 30 nm without the need to address the technical challenges of expensive next-generation lithography technologies such as EUV.

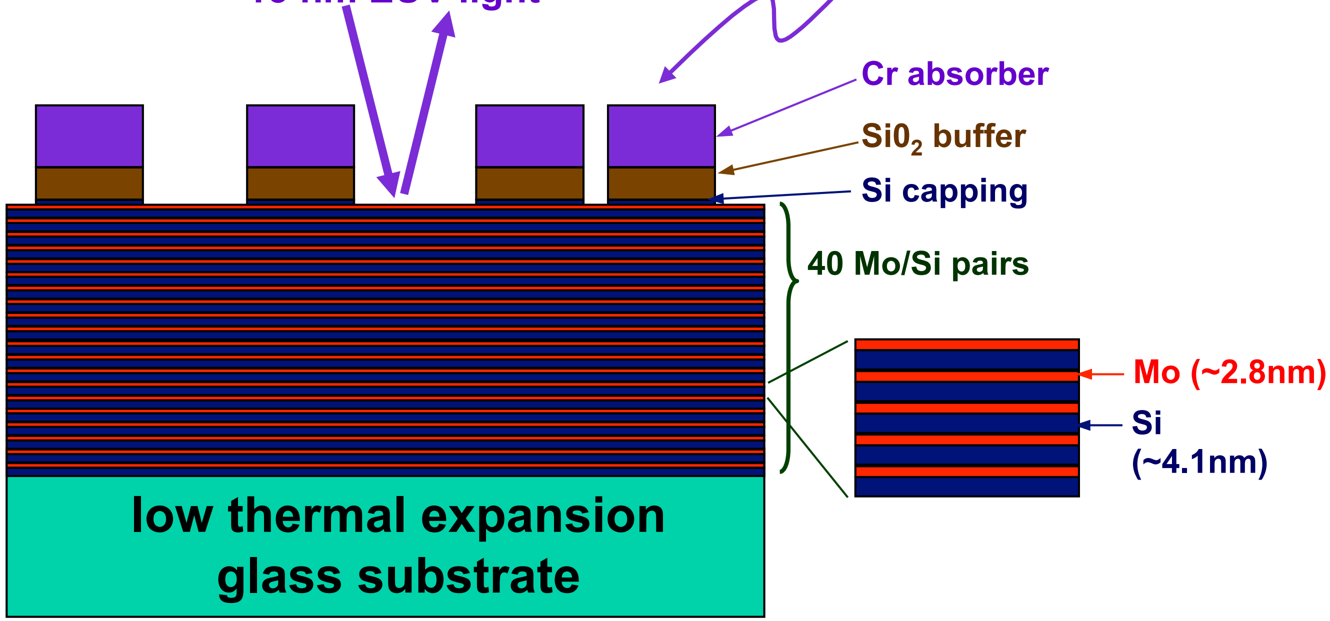
Even electron beam lithography may eventually require double patterning (due to secondary electron scattering) to achieve comparable half-pitch resolution, for instance, in the fabrication of 15 nm half-pitch X-ray zone plates.

EUV reflective mask

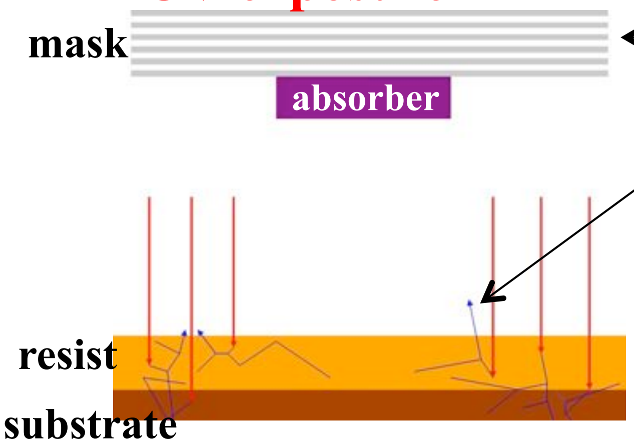
reticles



Intel EUV mask



EUV exposure



EUV multilayer and absorber (purple) constituting mask pattern for imaging a line.

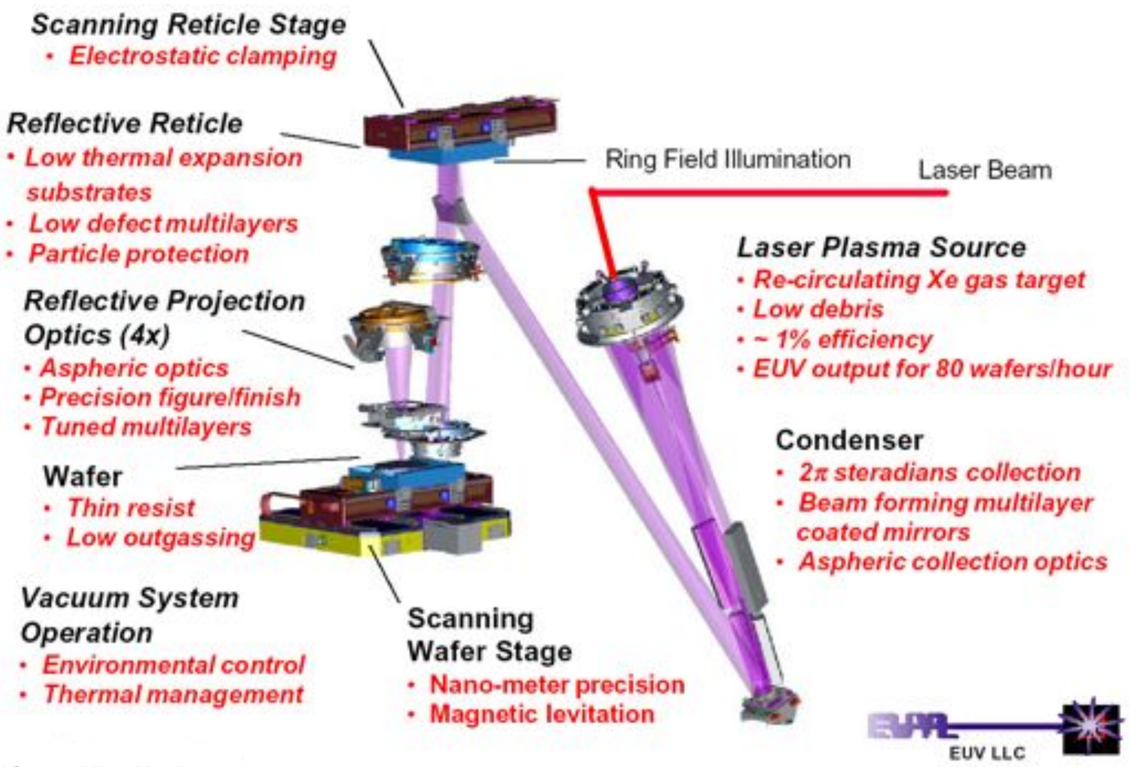
These electrons increase the extent of chemical reactions in the resist, beyond that defined by the original light intensity pattern.

As a result, a secondary electron pattern that is random in nature is superimposed on the optical image.

The unwanted secondary electron exposure results in loss of resolution, observable line edge roughness and linewidth variation.

EUV radiation (red) reflected from the mask pattern is absorbed in the resist (amber) and substrate (brown), producing photoelectrons and secondary electrons (blue).

EUV exposure tool



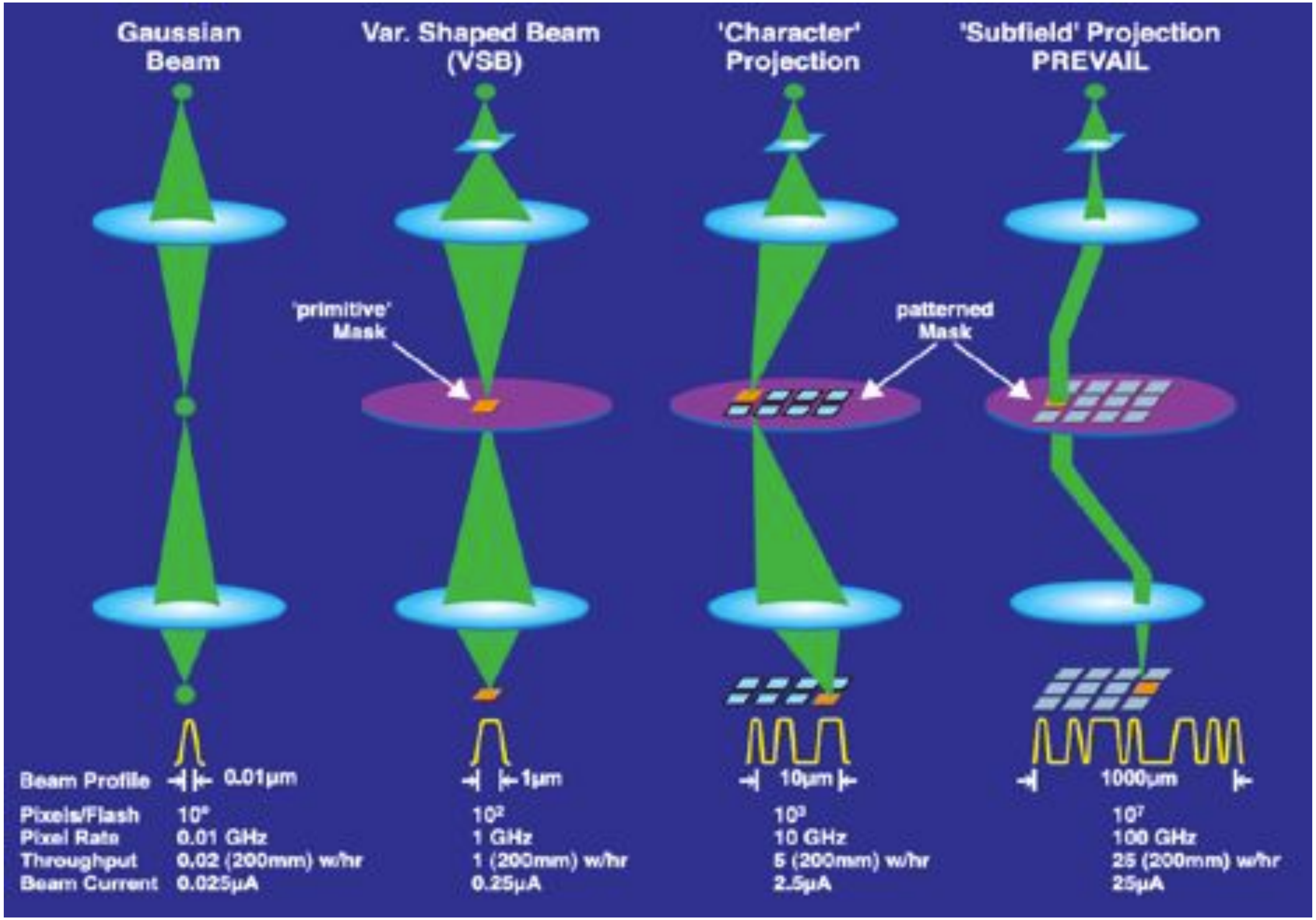
NXE:3100

- Uses very short 13.4 nm light
- 13.4 nm radiation absorbed by all materials
- Requires reflective optics coated with quarter-wave Bragg reflectors
- Uses reflective reticles with patterned absorbers
- Vacuum operation
- Unique source for EUV light

Intel Corporation & EUV LLC Charles (Chuck) W. Gwyn
Cahners MDR Microprocessor Forum 2000

22 February 2010: TSMC to purchase EUV lithography system from ASML

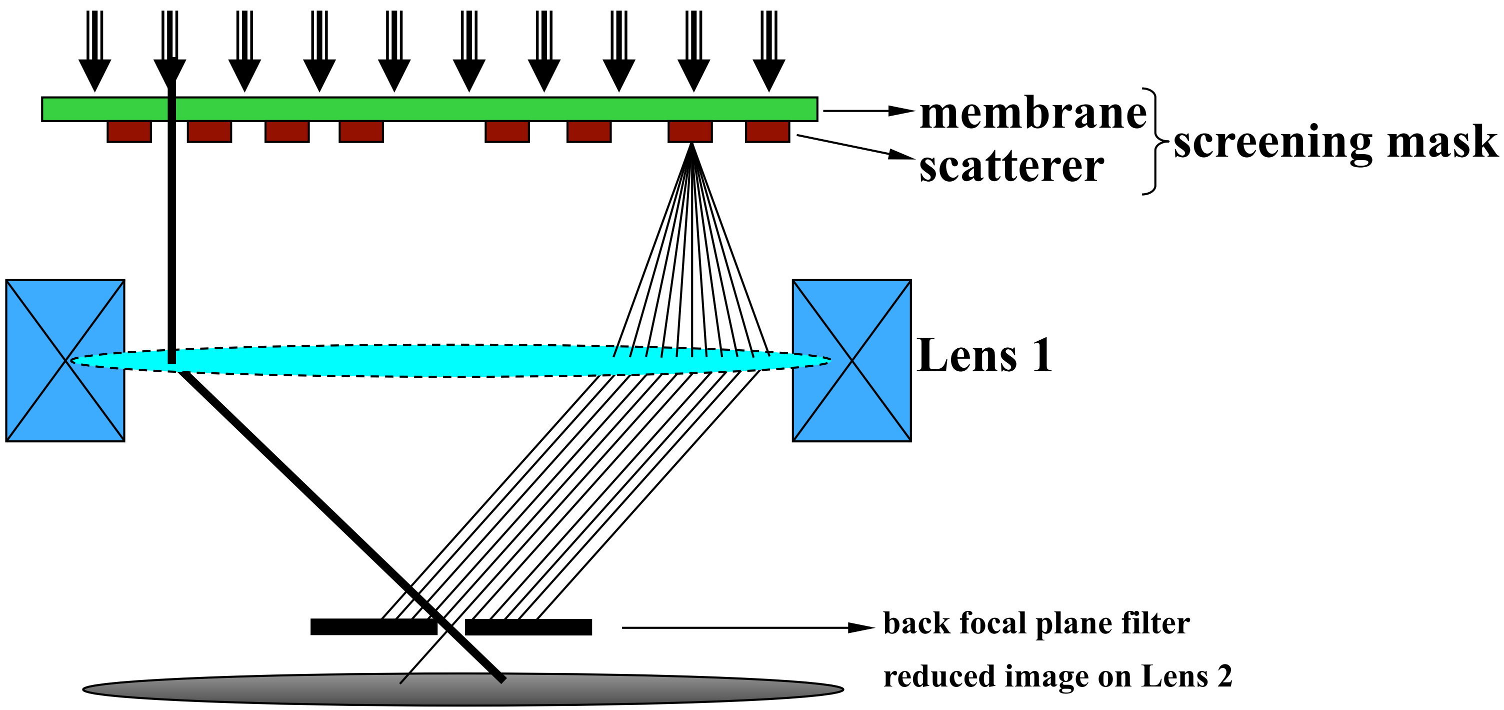
Electron Beam Lithography:



楊富量 (NDL), Outlook for 15nm CMOS Manufacture

Projection EBL Systems (SCALPEL):

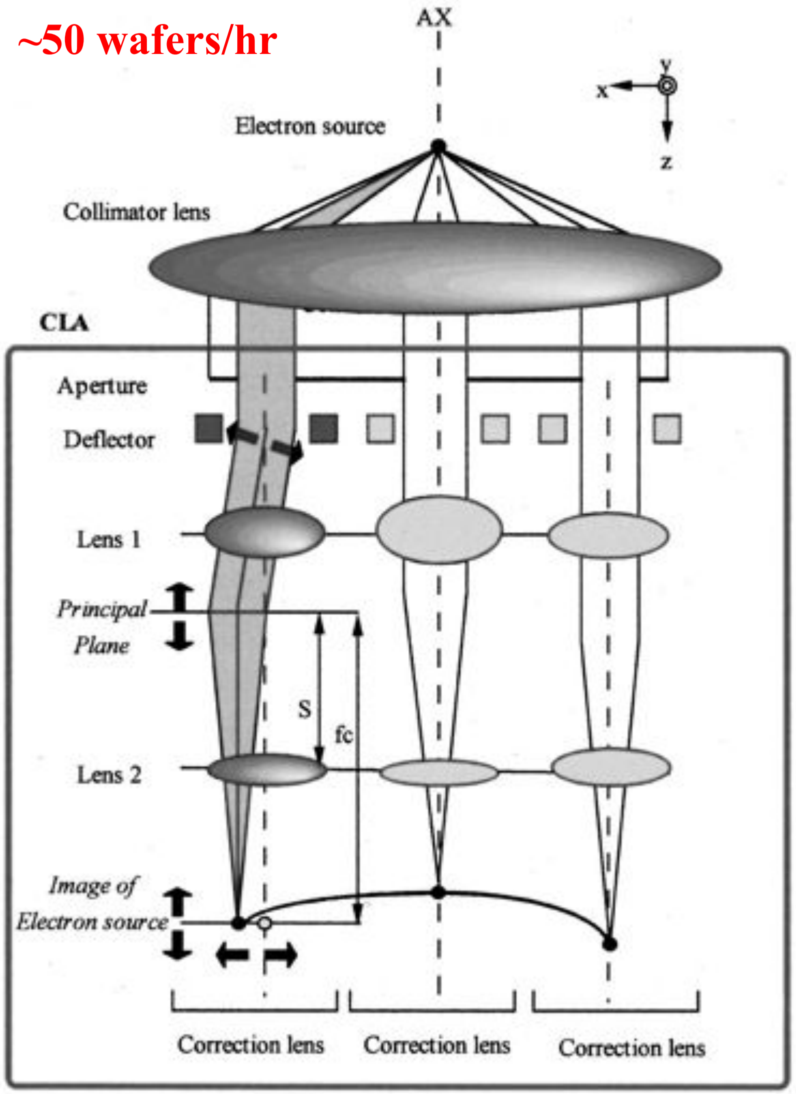
scattering with **a**ngular **l**imitation in **p**rojection **e**lectron beam **l**ithography



Multibeam direct-write electron beam lithography system

Single source with correction lens array

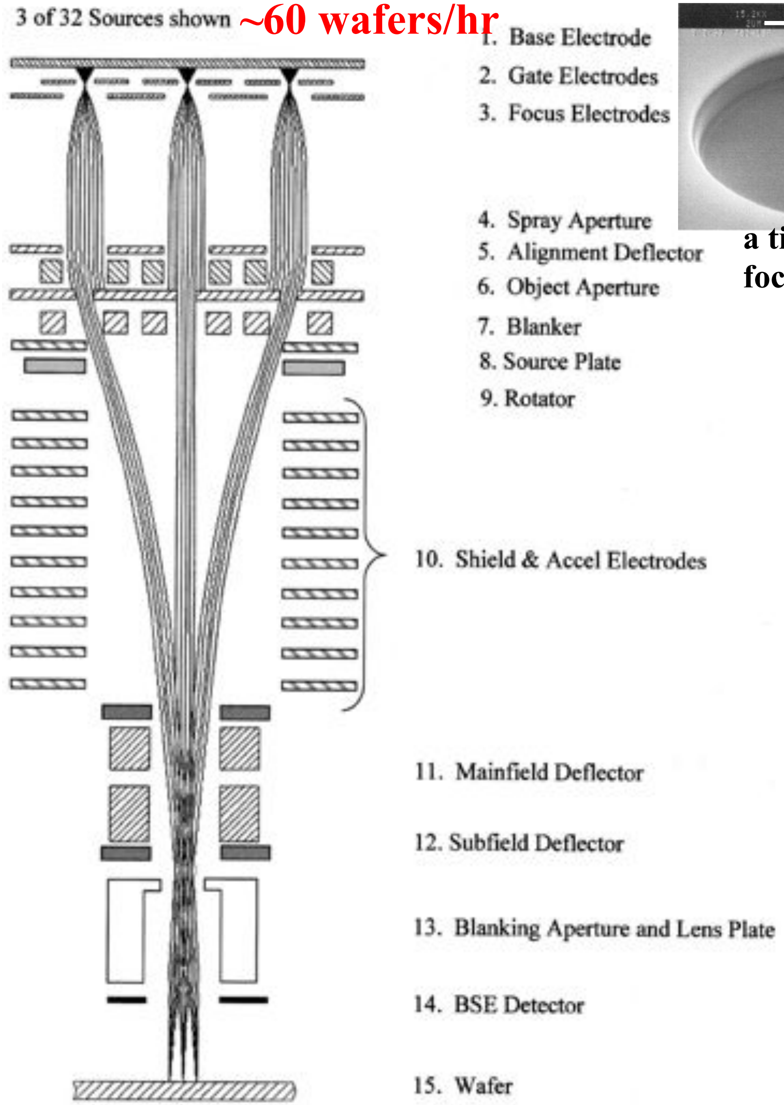
~50 wafers/hr

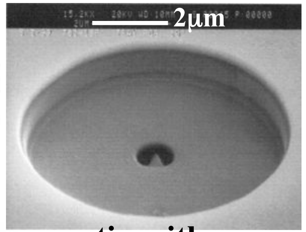


M. Muraki et al. J. Vac. Sci. Technol. B 18(6), 3061, 2000
Canon Inc.,

Multi-source with single electron optical column

~60 wafers/hr

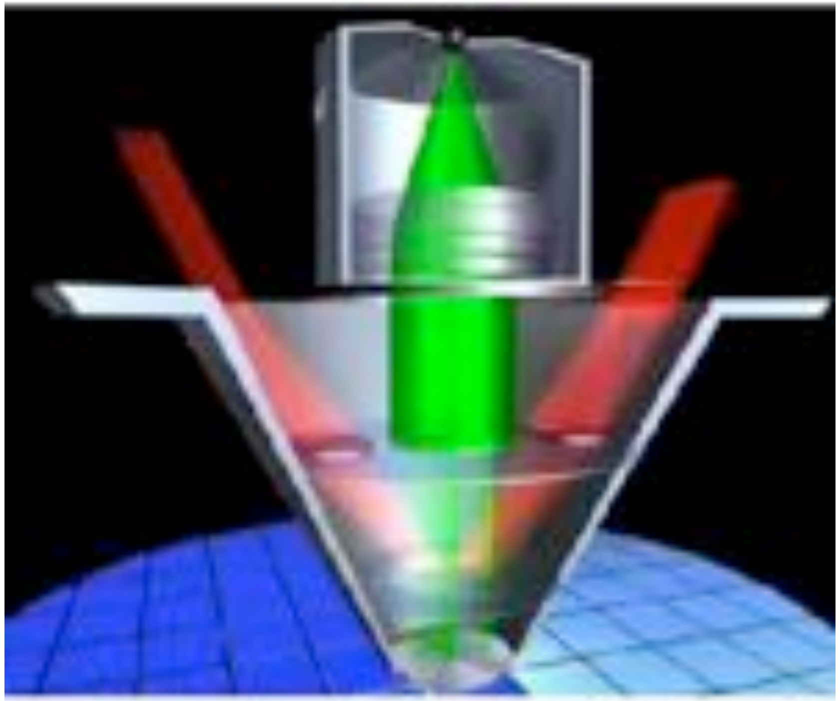




a tip with focus electrode

E. Yin et al. J. Vac. Sci. Technol. B 18(6), 3126, 2000
Ion Diagnostics Incorporated

Parallel E-Beam Lithography



MAPPER **(the manufacturer)**

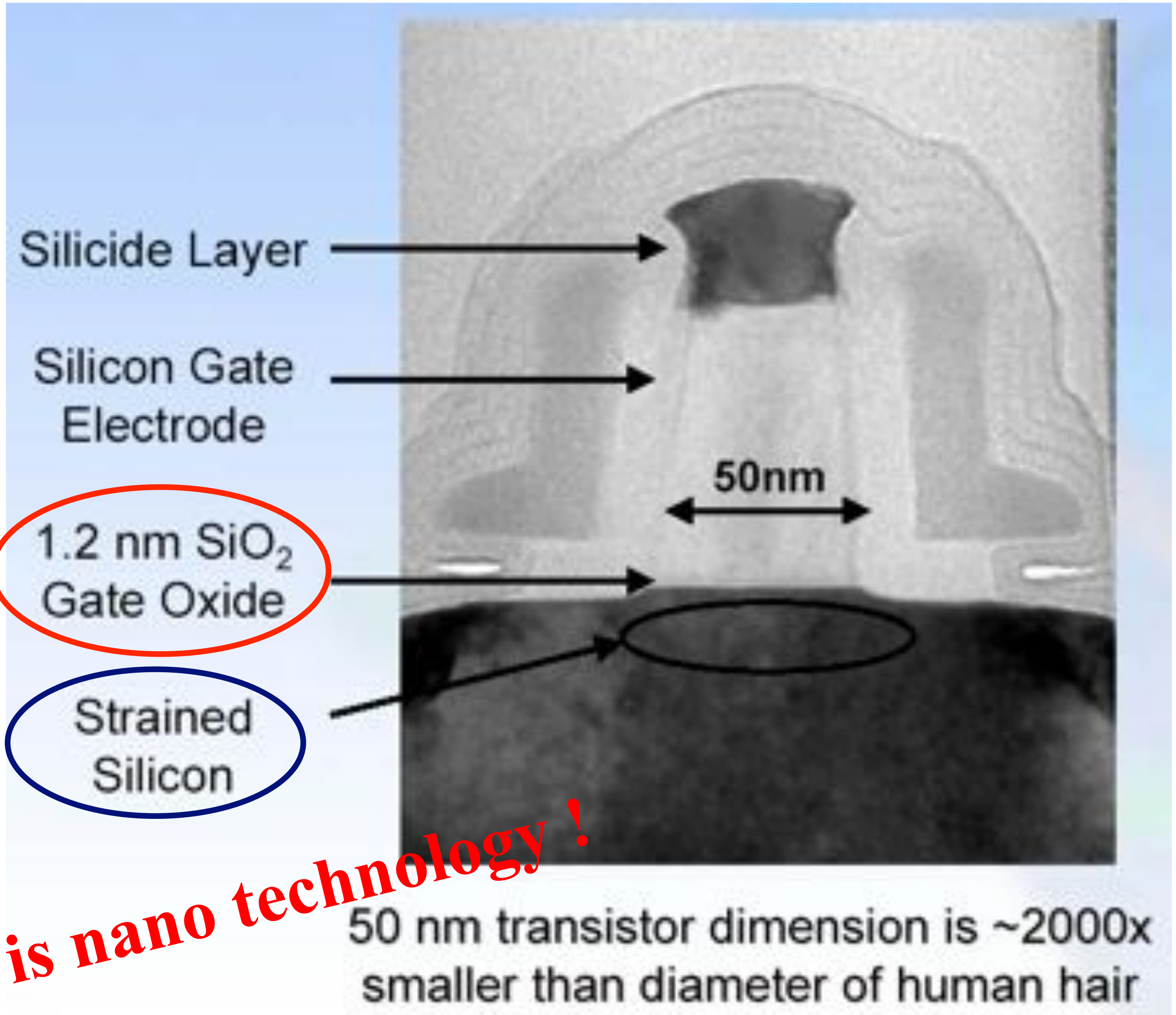
More than 10,000 parallel electron beams.

Fibre-optics is capable of transporting a large quantity of information.

In October 2008, Mapper and Taiwan Semiconductor Manufacturing Co. have signed an agreement, according to which Mapper will ship its first 300mm multiple-electron-beam maskless lithography platform for process development and device prototyping to TSMC.

Material Engineering gains importance !

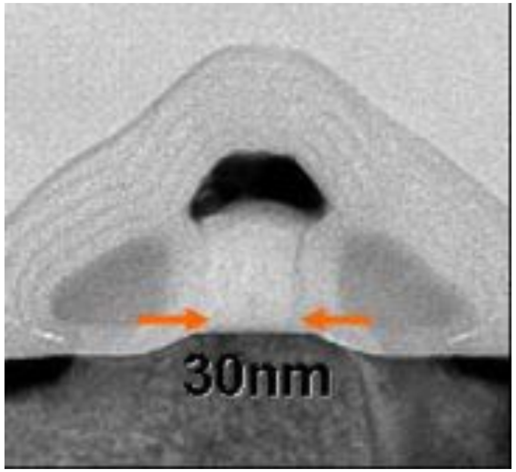
90 nm Generation Transistor



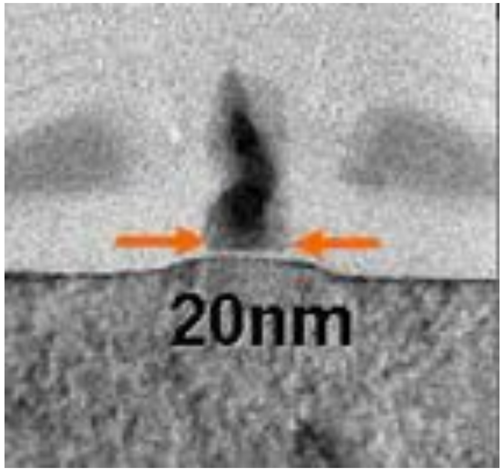
This is nano technology !

source: Intel develop forum
Spring, 2003

Experimental transistors for future process generations

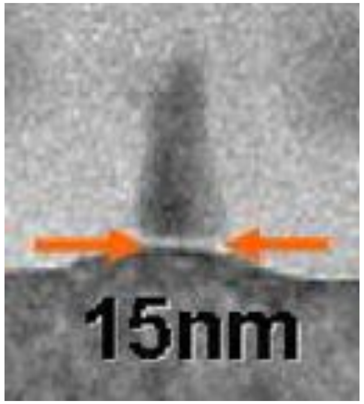


65nm process
2005 production

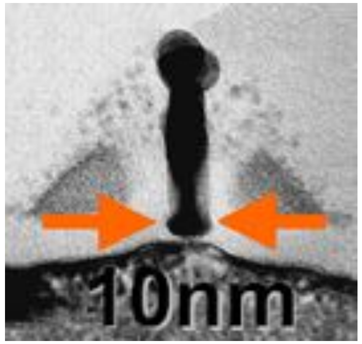


45nm process
2007 production

CMOS
0.8 nm conventional gate oxide



32nm process
2009 production



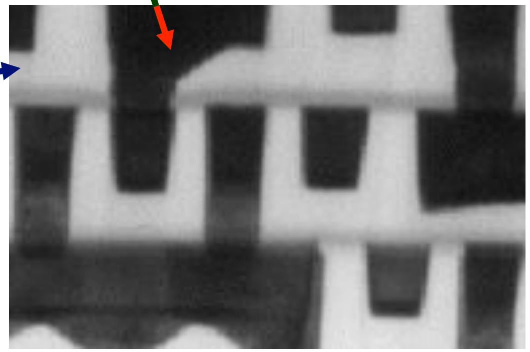
22nm process
2011 production

Intel C. Michael Garner Sept. 2003 NanoSIG

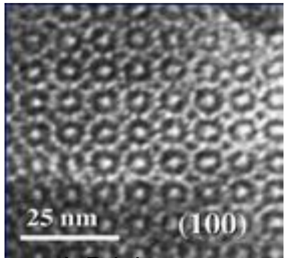
Nano materials will play an important role in the silicon nanotechnology platform

Interconnectors with high electrical conductivity

Low K interlevel Dielectric

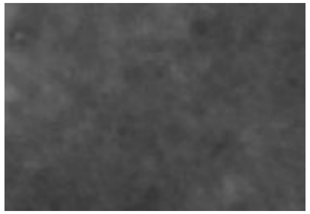


High K gate oxide

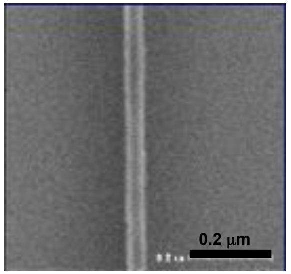


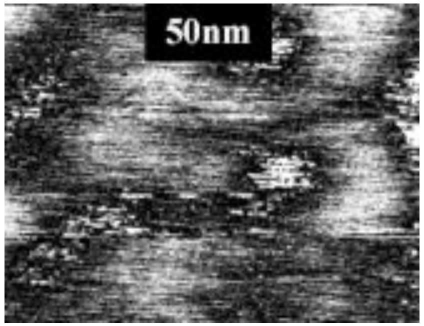
J. Brinker,
UNM/Sandia National Labs

Strained Si



Photoresist





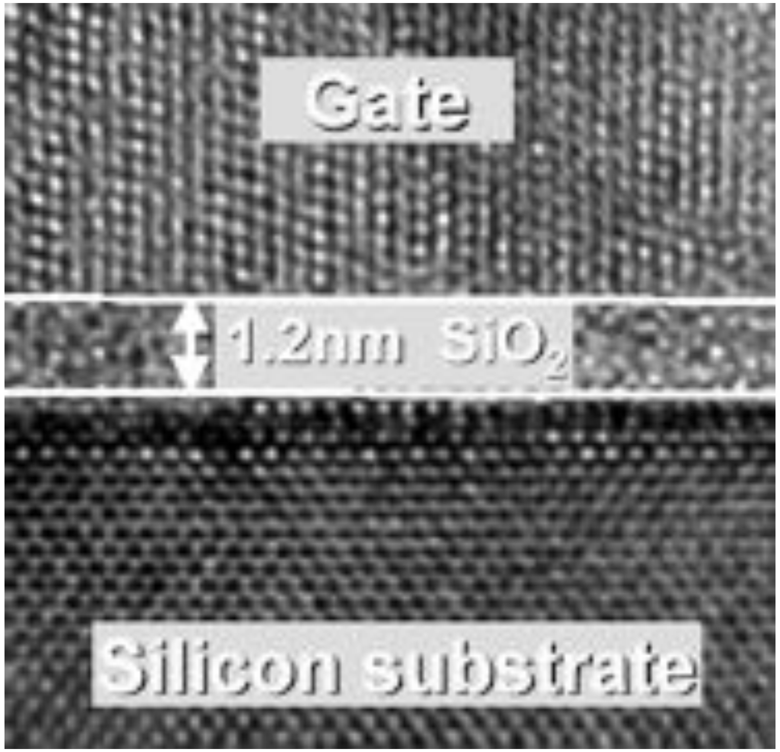
C. Michael Garner, Intel, Sept.16, 2003

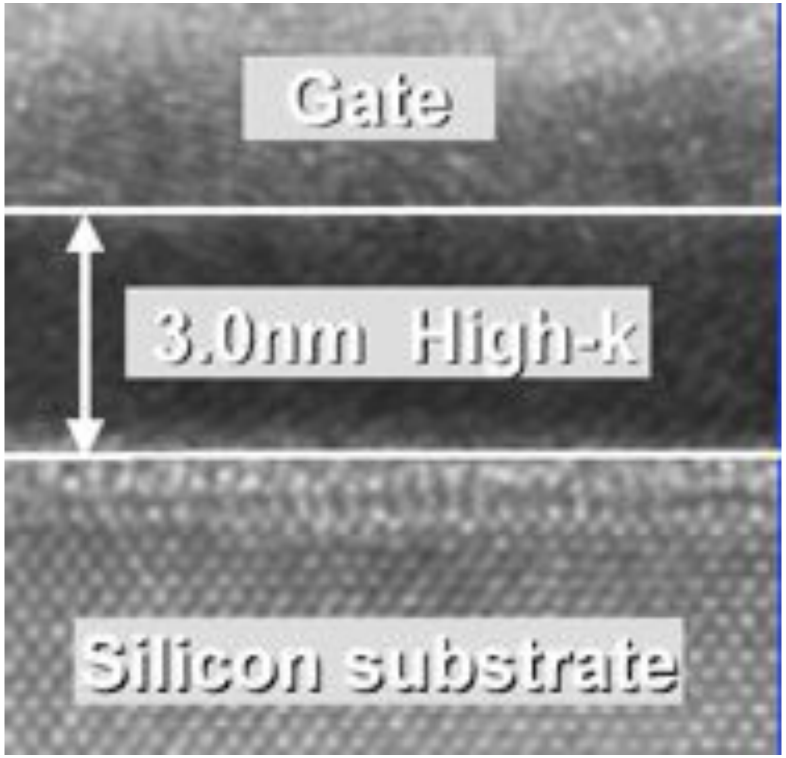
Introduction of new materials

1st Production	1997	1999	2001	2003	2005	2007	2009	2011
Process Generation	0.25μm	0.18μm	0.13μm	90 nm	65 nm	45 nm	32 nm	22 nm
Wafer Size (mm)	200	200	200/ 300	300	300	300	300	300
Inter-connect	Al	Al	Al	Cu	Cu	Cu	Cu	?
Channel	Si	Si	Si	Strained Si	Strained Si	Strained Si	Strained Si	Strained Si
Gate dielectric	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	High-k	High-k	High-k
Gate electrode	PolySi	PolySi	PolySi	PolySi	PolySi	Metal	Metal	Metal

source: Intel develop forum

Introduction of high-K gate dielectric





	90 nm process	Experimental high-K
Capacitance	1X	1.6X
Leakage	1X	<0.01X

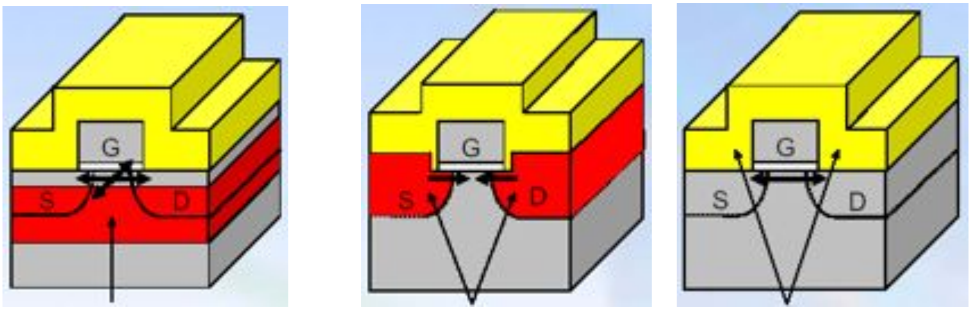
Carolyn Block, Intel 2003

A message from Intel

Compress P-doped regions
by filling SiGe into carved trenches,
hole conduction increased by 25%

Stretch N-doped regions
by annealing SixNy cover layer,
electron conduction increased by10%

Traditional MOS **new PMOS** **new NMOS**

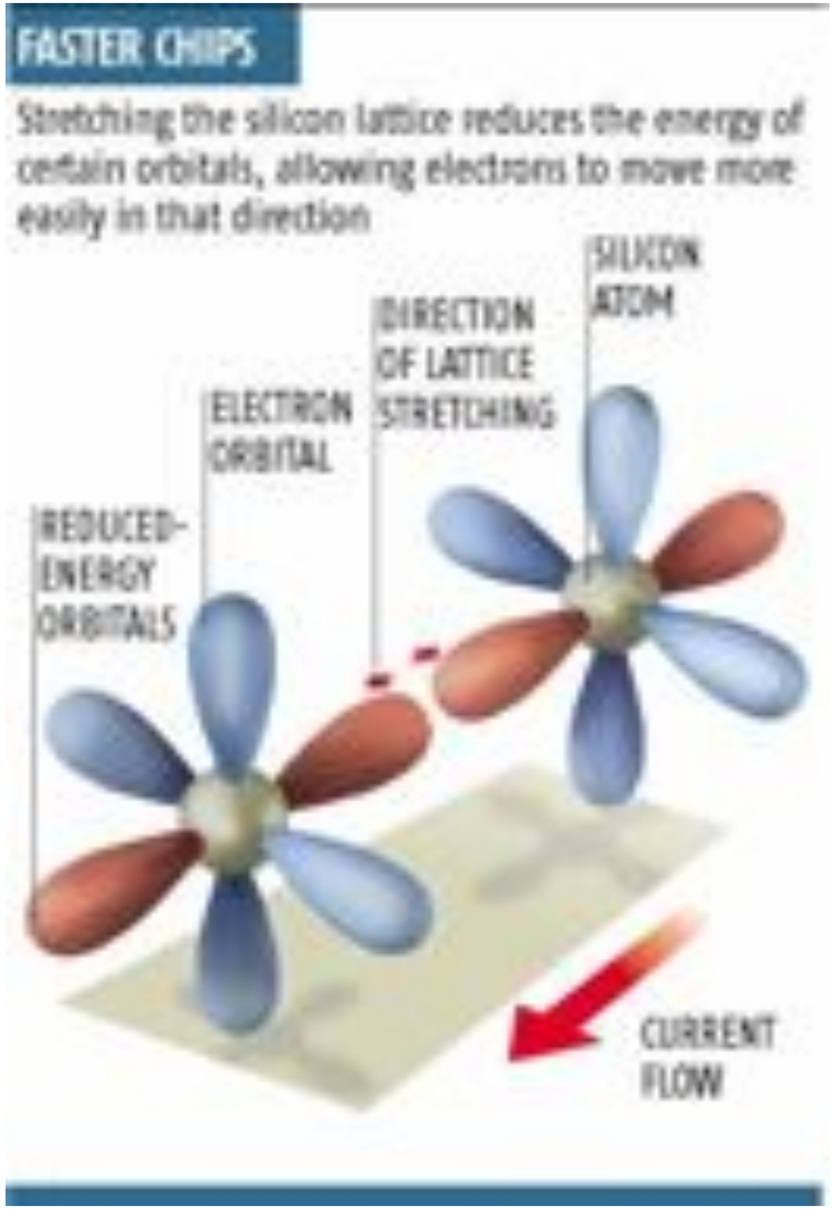


Graded SiGe layer **Selective SiGe S-D** **Tensile Si_3N_4 Cap**

Strained silicon benefits

- **Strained silicon lattice increases electron and hole mobility**
- **Greater mobility results in 10-20% increase in transistor drive current (higher performance)**
- **Both NMOS and PMOS transistors improved**

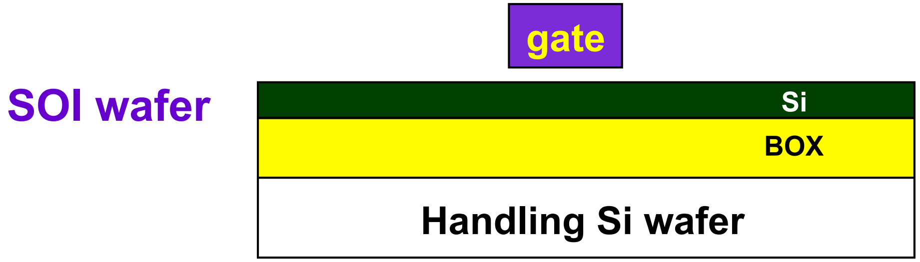
Intel develop forum



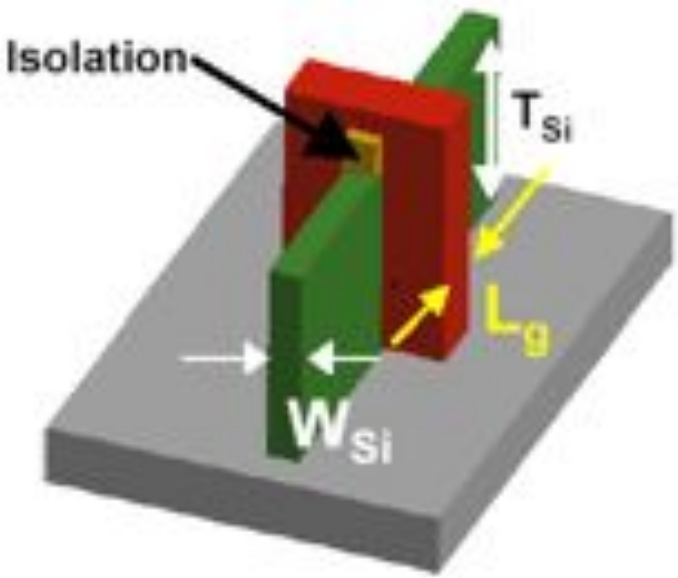
http://www.newscientist.com/news/news.jsp?id=ns99994493

2003-12-20

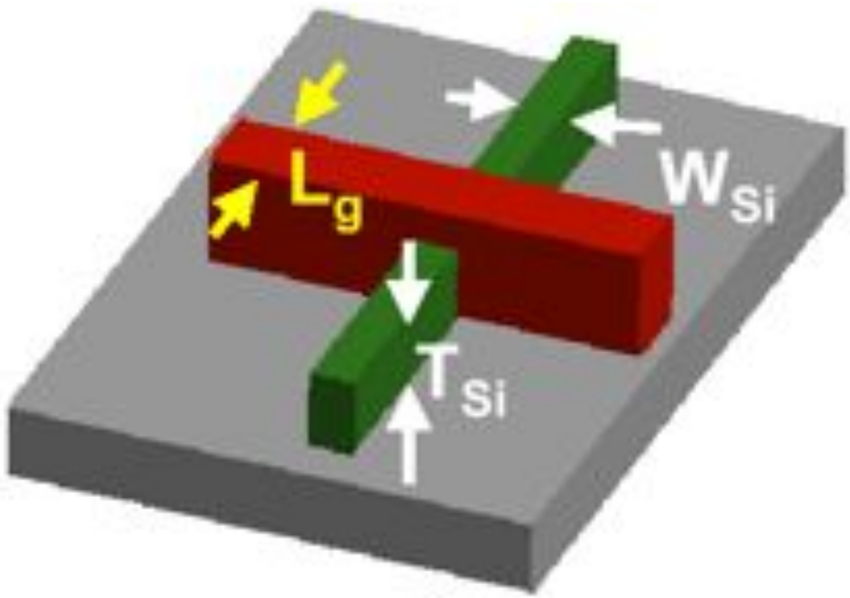
Three types of new Fully Depleted Transistors



Planar fully depleted SOI

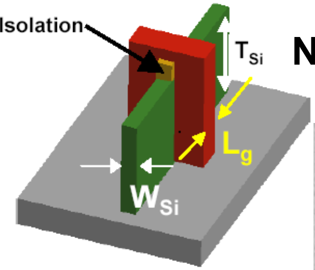


Non-planar Double-gate (FinFET)

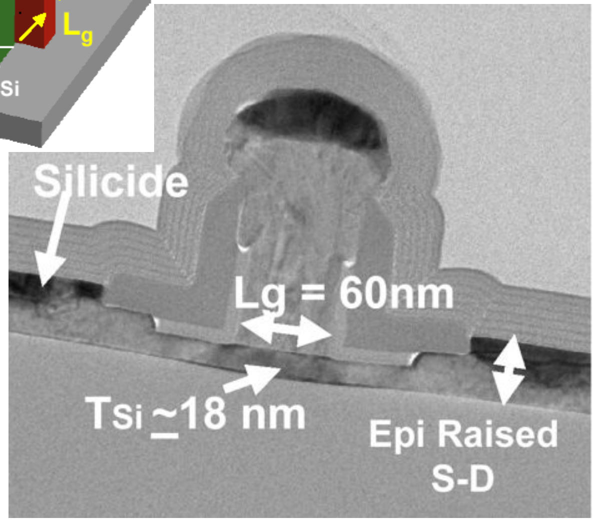


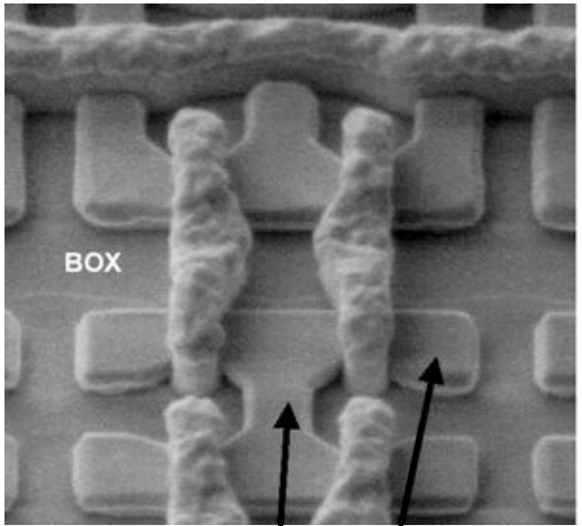
Non-planar Tri-gate

Fully Depleted Transistors made on SOI wafers



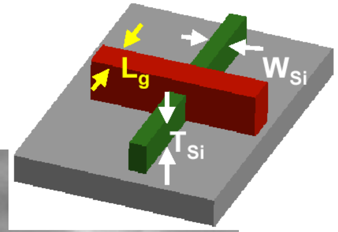
Non-planar Double-gate (FinFET)

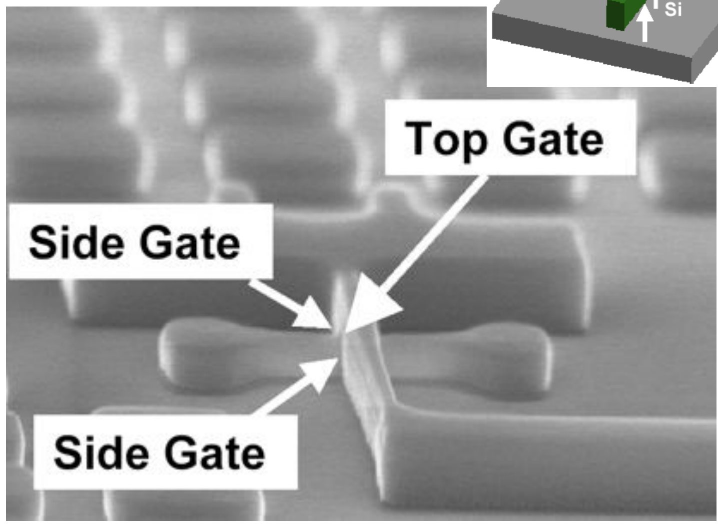


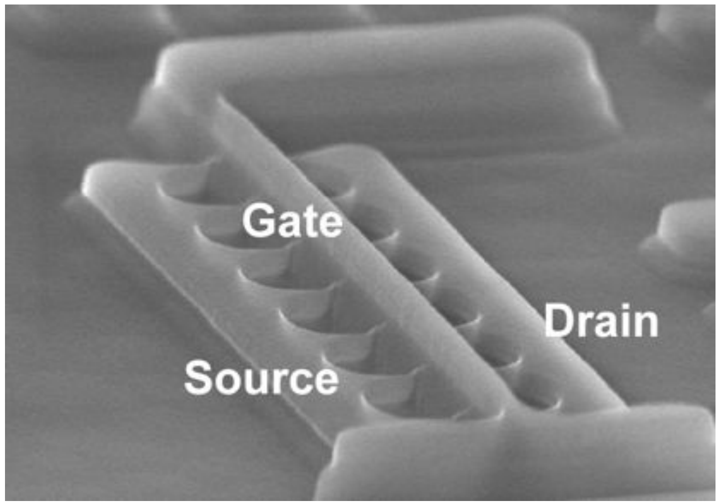


Raised S-D using Selective Epi-Si Deposition

Non-planar Tri-gate



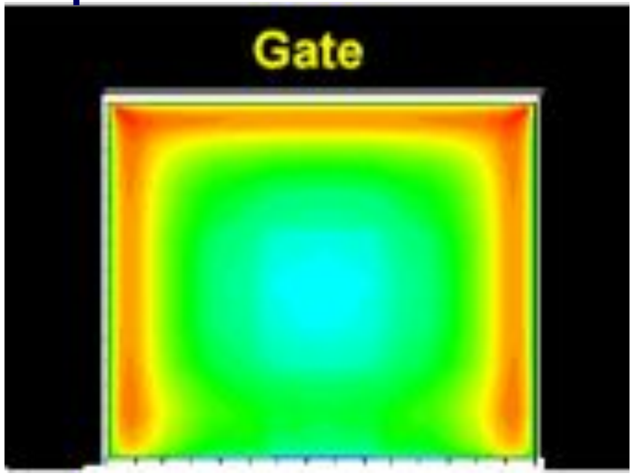


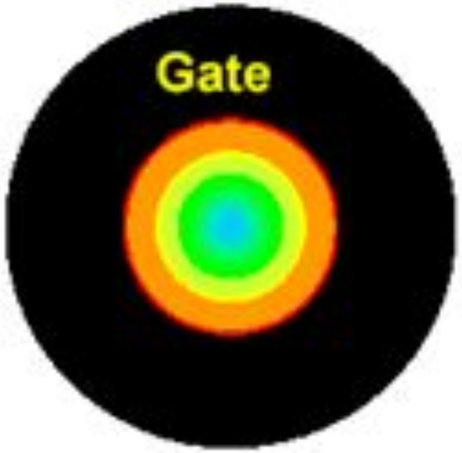


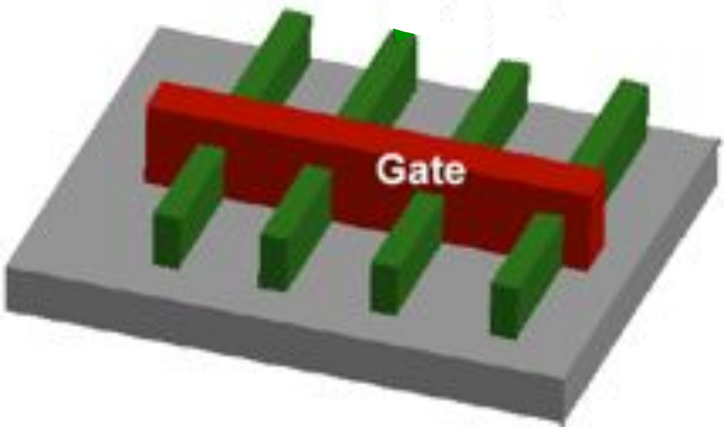
Robert Chau, Intel, 61st Device Research Conference June 2003

From Tri-gate transistors to Nano-wire transistors

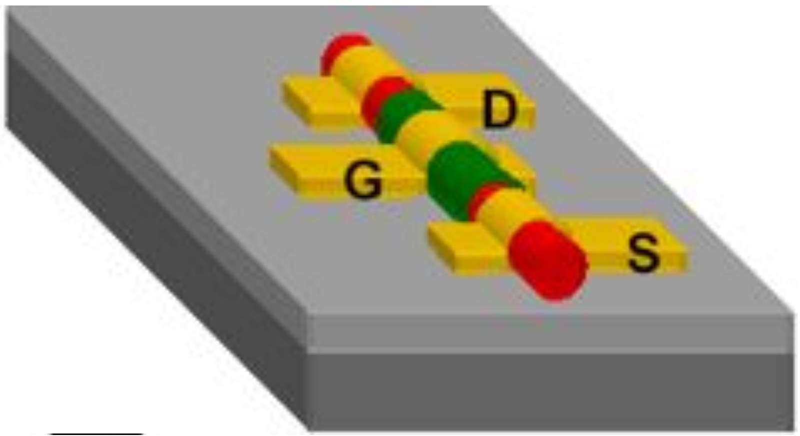
depletion electric field







Tri-gate transistor



Nano-wire transistor