Introduction to Nanotechnology

- Textbook：
  Nanophysics and Nanotechnology
  by:
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Classroom: A209
Time: Thursday; 13:40-16:30 PM
Office hour: Thur. 10:00-11:30 AM or by appointment

What are limits to smallness

1. Particles

Atoms → ~ 0.1 nm

Photons → Particles of light

E: hv

hv → Light frequency in Hz

h → Planck's constant : 6.6x10-34 J.s

Molecules → Combine of at least two atoms

Subjects: Today class

1. Top Down and Bottom Up Approach
2. Silicon Technology
3. Patterning, Masks
4. Etching Technology; Dry and Wet
5. Photo-lithography
6. Chemical Vapor Deposition (CVD)
7. Sputtering

Nanofabrication is used in:

- Information storage
- Opto-electronics
- Sensors
- Micro-electro-mechanical (MEMs) devices
- Power semiconductors
- Pharmaceuticals
- Bio-medical applications
- Microelectronics (chips)

Device Fabrication Technology

About 10^{20} transistors (or 10 billion for every person in the world) are manufactured every year.

VLSI (Very Large Scale Integration)
ULSI (Ultra Large Scale Integration)
GSI (Giga-Scale Integration)

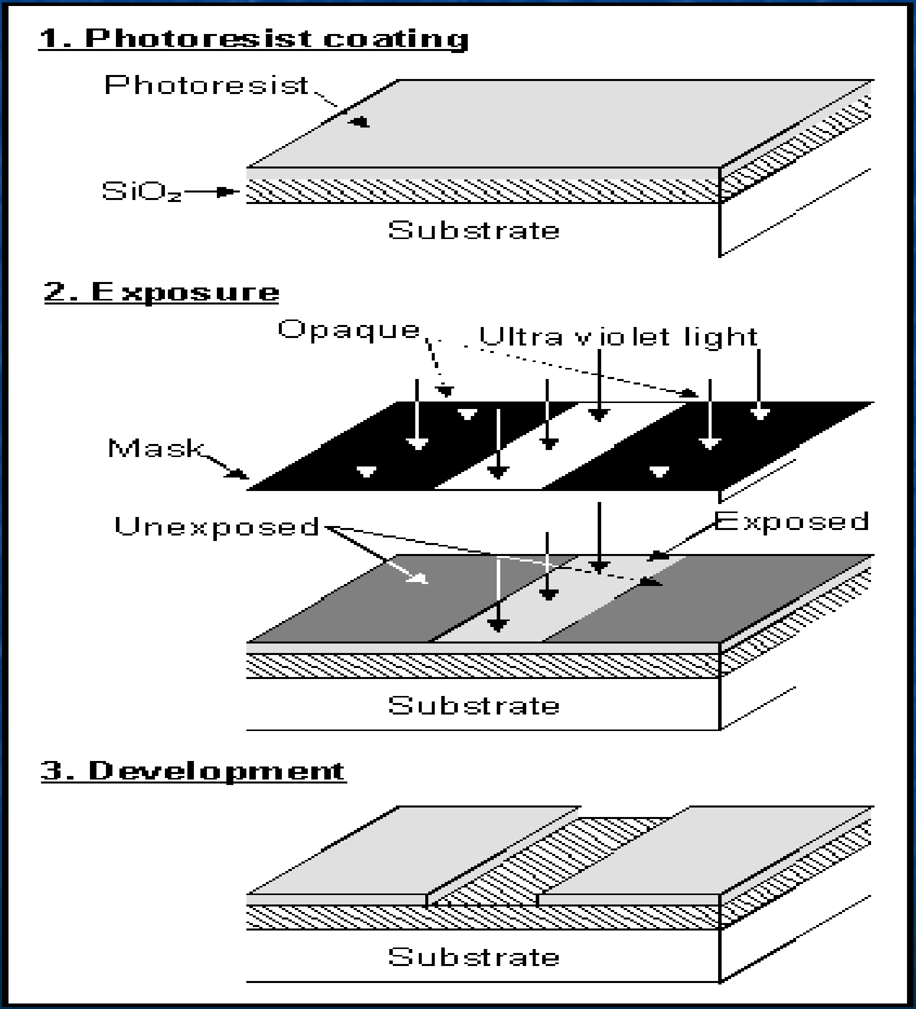
Variations of this versatile technology are used for flat-panel displays, micro-electro-mechanical systems (*MEMS*), and chips for DNA screening...

Top-down and Bottom-up

Processes

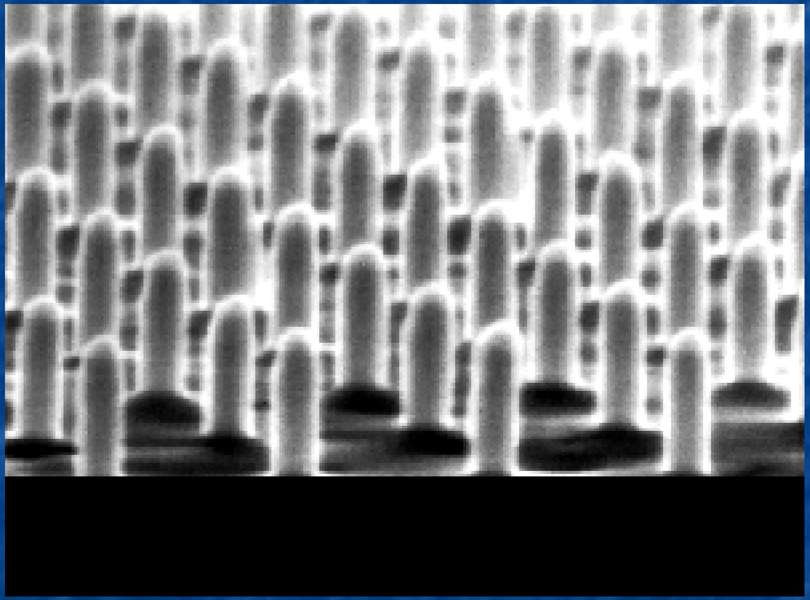
Top-Down Approach

- Uses the traditional methods to pattern a bulk wafer as in EE 418 lab.
- Is limited by the resolution of lithography.



What Constitutes a Top-down Process?

- Adding a layer of material over the entire wafer and patterning that layer through photolithography.
- Patterning bulk silicon by etching away certain areas.



Problems with the Top-down Process

- Cost of new machines and clean room environments grows exponentially with newer technologies.
- Physical limits of photolithography are becoming a problem.
- With smaller geometries and conventional materials, heat dissipation is a problem.

Bottom-Up Approach

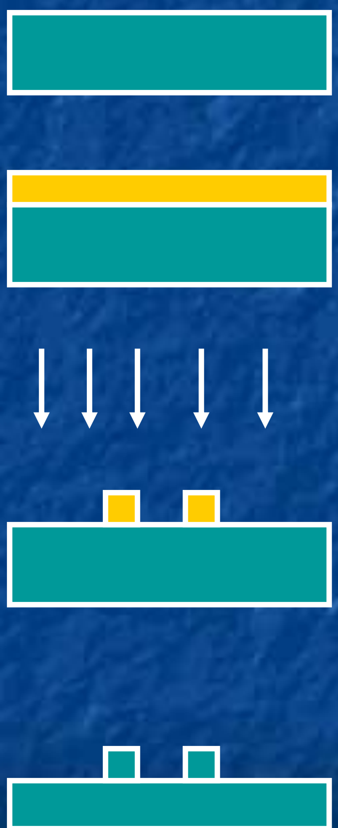
- The opposite of the top-down approach.
- Instead of taking material away to make structures, the bottom-up approach selectively adds atoms to create structures.

The Ideas Behind the Bottom-up Approach

- Nature uses the bottom up approach.
  - Cells
  - Crystals
  - Humans
- Chemistry and biology can help to assemble and control growth.

Top-down Versus Bottom-up

Top Down Process



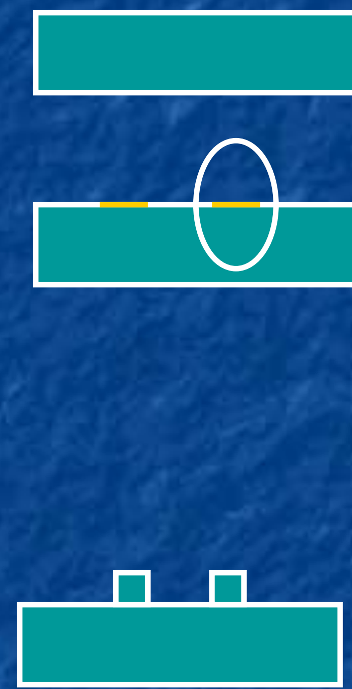
Start with bulk wafer

Apply layer of photoresist

Expose wafer with UV light through mask and etch wafer

Etched wafer with desired pattern

Bottom Up Process



Start with bulk wafer

Alter area of wafer where structure is to be created by adding polymer or seed crystals or other techniques.

Grow or assemble the structure on the area determined by the seed crystals or polymer. (self assembly)

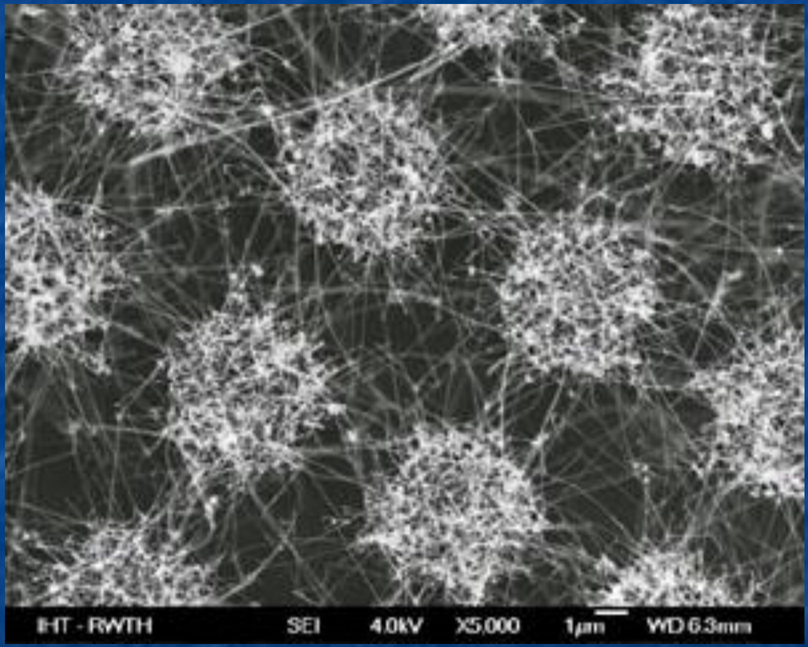
Similar results can be obtained through bottom-up and top-down processes

Why is Bottom-Up Processing Needed?

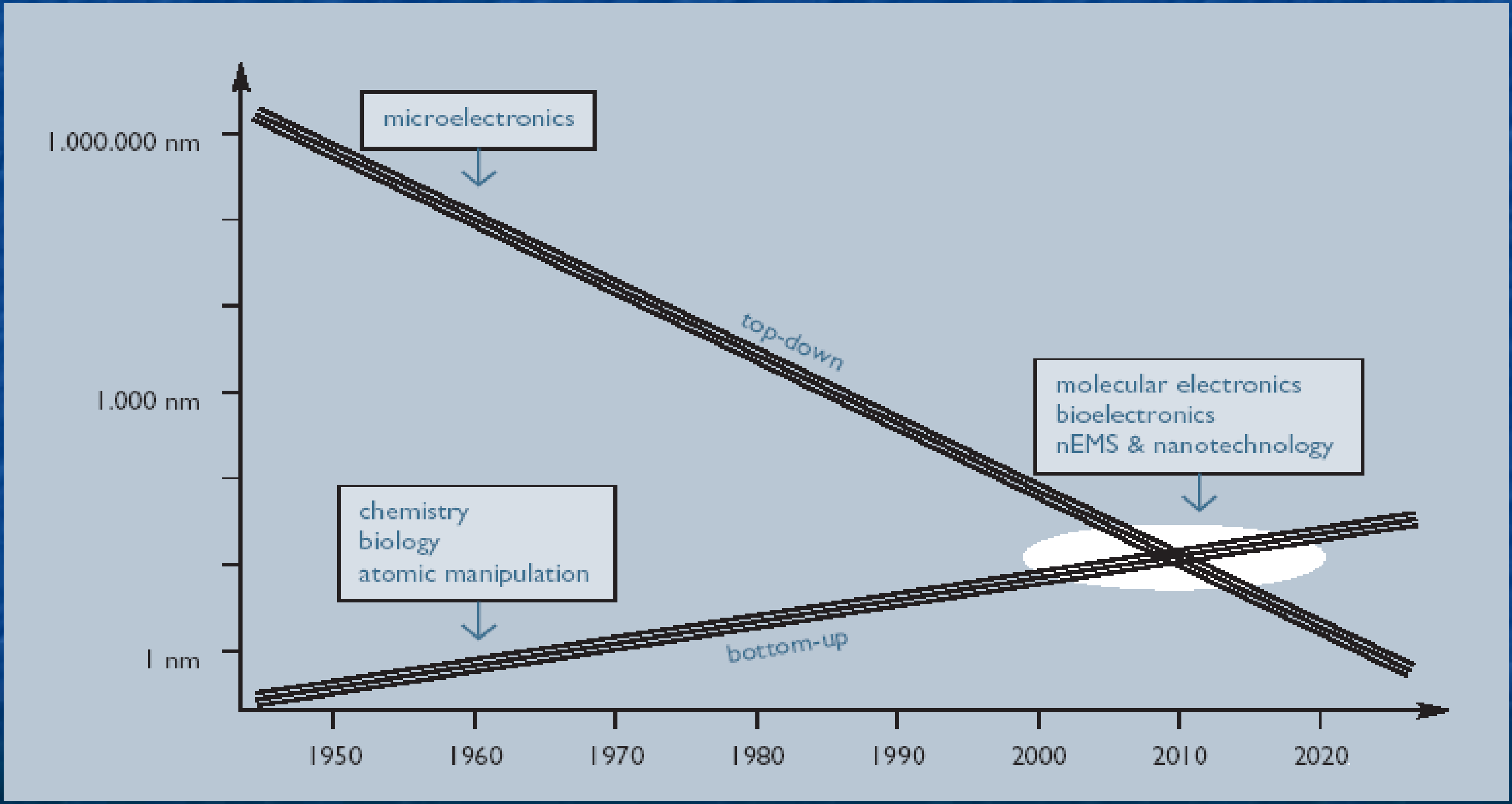
- Allows smaller geometries than photolithography.
- Certain structures such as Carbon Nanotubes and Si nanowires are grown through a bottom-up process.
- New technologies such as organic semiconductors employ bottom-up processes to pattern them.
- Can make formation of films and structures much easier.
- Is more economical than top-down in that it does not waste material to etching.

Applications of Bottom-Up Processing

- Self-organizing deposition of silicon nanodots.
- Formation of Nanowires.
- Nanotube transistor.
- Self-assembled monolayers.
- Carbon nanotube interconnects.



Future of Top-down and Bottom-Up Processing



Challenges for the Bottom-Up Approach

- Making sure that the structures grow and assemble in the correct way.
- Forming complex patterns and structures using self assembly.
- Contamination has a significant impact on devices with such small geometries.
- Fabricating robust structures.

Strategies for Bottom-Up Processing

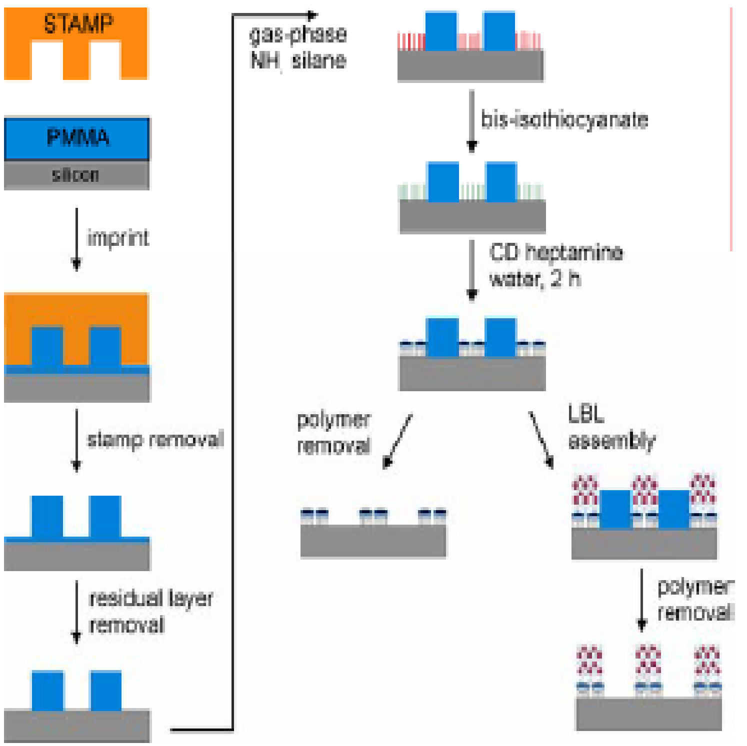


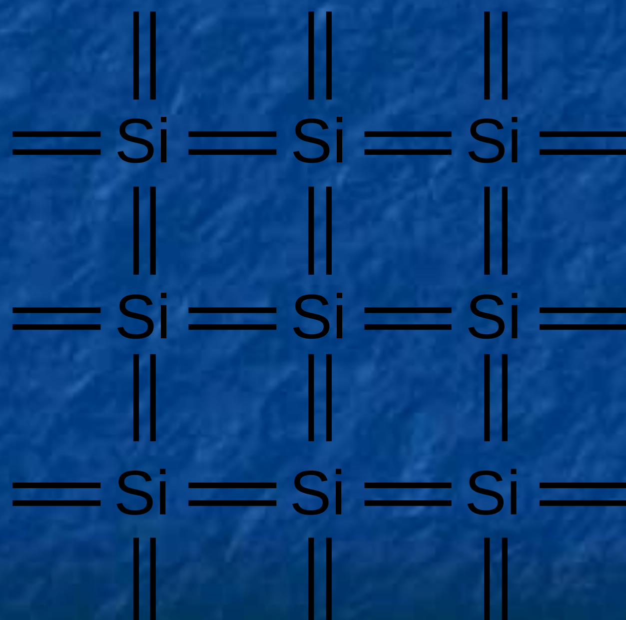
Figure 1. Integrated nanofabrication scheme incorporating nanoimprint lithography and layer-by-layer assembly.

- Combination of top-down and bottom-up processes to simplify construction.
- Use catalysts and stresses to achieve more one-directional growth.

- Top-down processing has been and will be the dominant process in semiconductor manufacturing.
- Newer technologies such as nanotubes and organic semiconductors will require a bottom-up approach for processing.
- Self-assembly eliminates the need for photolithography.
- Bottom-up processing will become more and more prevalent in semiconductor manufacturing.

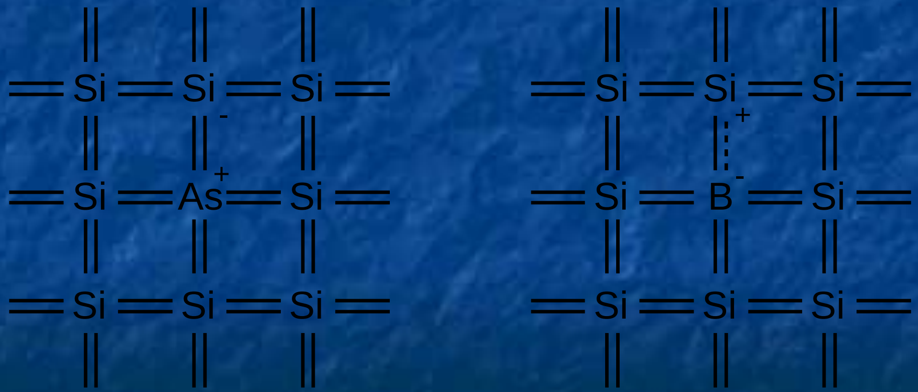
Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)

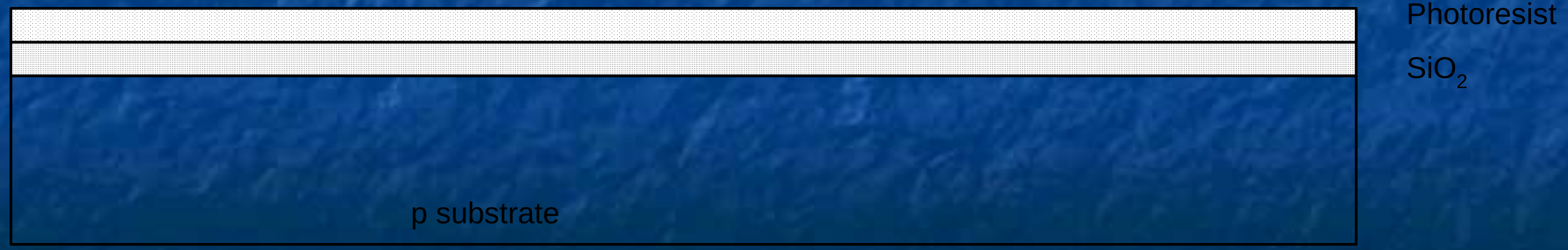


Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace

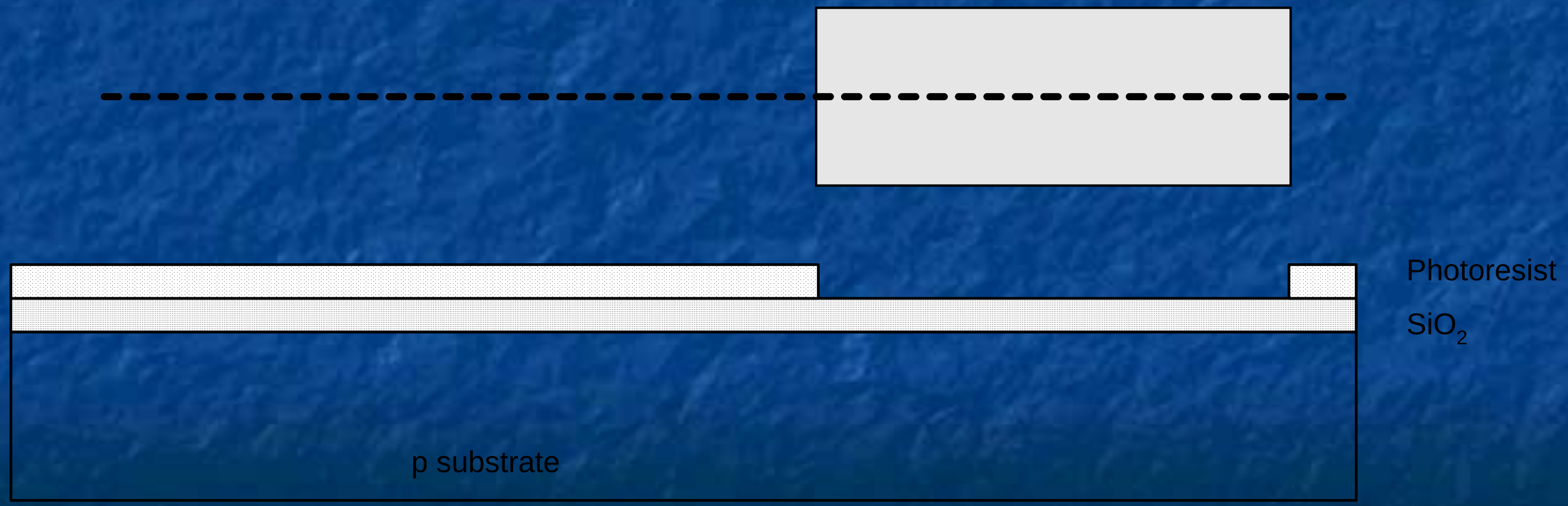
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



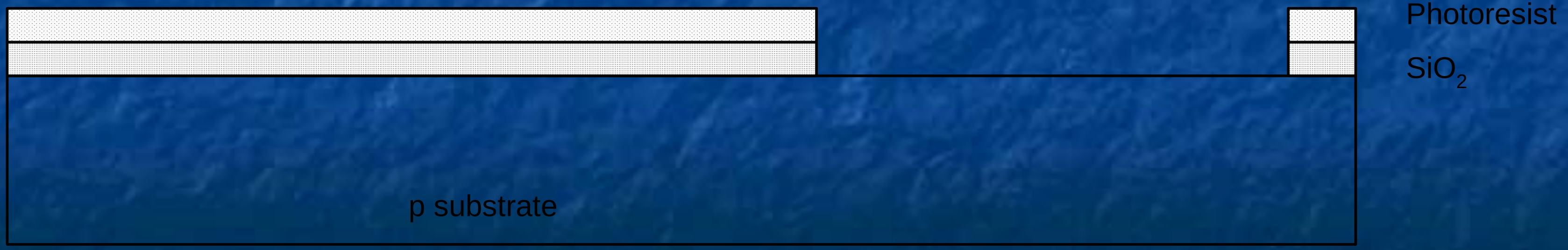
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



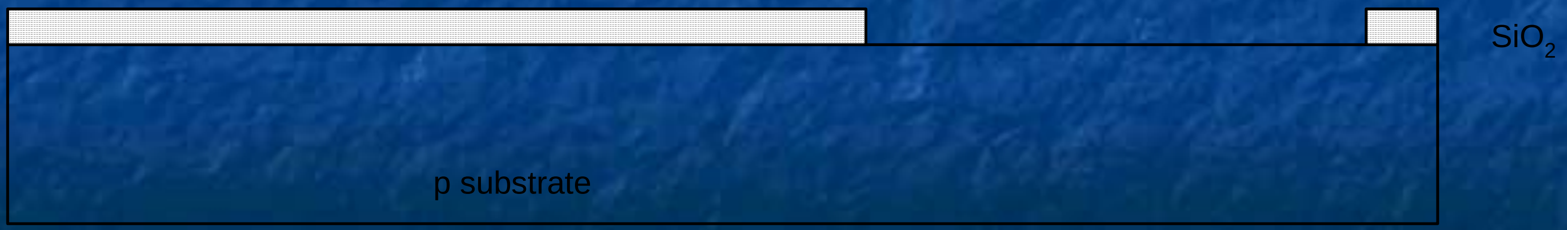
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step



Pattern Transfer Techniques: Results

1. Etching Processes

Fluorine Beam

Transfer mask pattern via etching into substrate for ordered arrays of trenches.

Ion Beam

Transfer mask pattern via ion etching into substrate for ordered arrays of trenches or pillars.

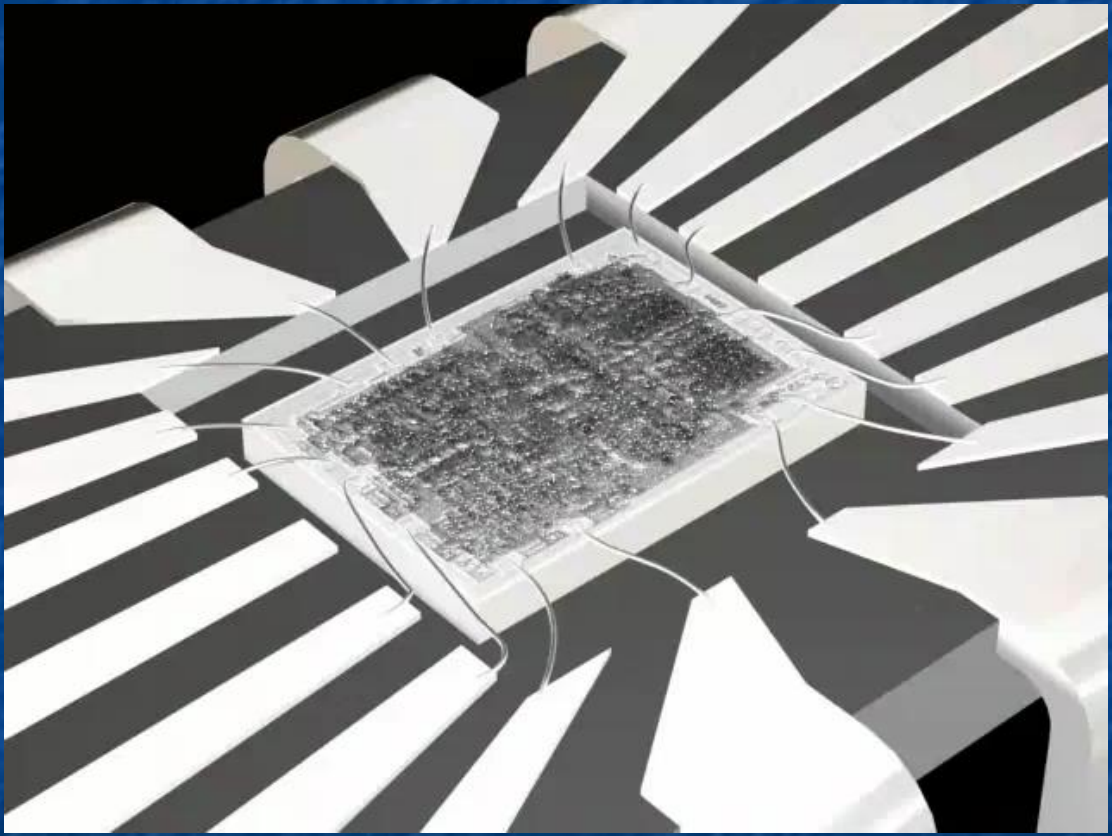
2. Growth Processes

Sputtering and Thermal Deposition

Transfer mask pattern via deposition onto substrate for ordered arrays of dots.

Microfabrication

Microfabrication . . . that's how you make integrated circuits, right?



But how is all of this done?

For very good reasons, it is sometimes called "micro-machining"

Classic Machining: 1) Start with big block of metal

2) "Machine" away parts you don't want

Use variety of lathe bits, mills and drills

But all are basically scraping & gouging away material

Micro-machining: 1) Start with Silicon wafer (~ 1/4 mm thick, up to 300 mm diameter)

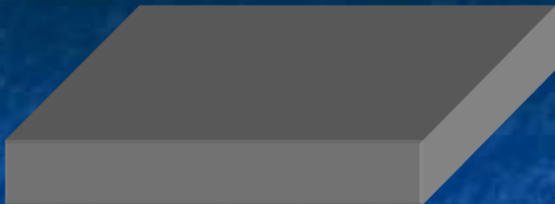
2) Spray on or grow on additional layer

3) Apply, expose, develop pattern in photographic emulsion

4) Etch or blast away material not protected by emulsion

5) Strip off emulsion → Cycle back to step 2

Schematically:



:Starting substrate

:Deposit layer of desired material

Deposit photographic emulsion:

Expose photographic emulsion:

Schematically (cont'd):

:Develop photographic emulsion

Etch desired materal:

Remove photographic emulsion:

After SEVEN steps, finally get desired 3D shape of new material!

BUT CAN DO THIS SIMULTANEOUSLY AT A BILLION DIFFERENT POINTS!!

Or going over that a little more slowly:

Step 1) Start with Silicon wafer

Silicon, element 14 in the periodic table, is known as a semiconductor:

- Insulators: Electrons held so strongly in bonds they can't move around

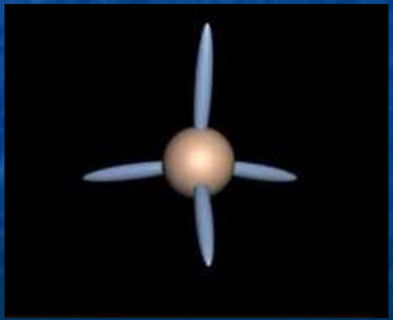
- Conductors (metals): Electron bonds so weak, electrons wander everywhere

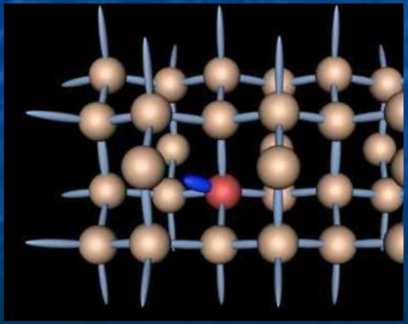
- Semiconductor: Electrons can escape bonds (w/ heat)

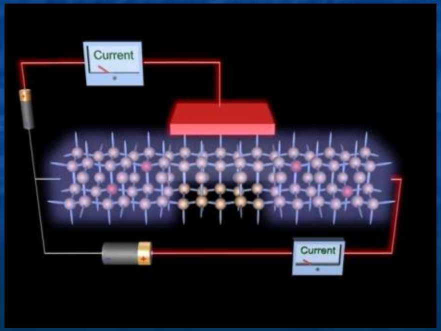
  or

  Extra non-bonding electrons can be added via impurity atoms

For details see "UVA Virtual Lab" webpage on How Semiconductors and Transistors Work







It really isn't electronic properties that make silicon so special:

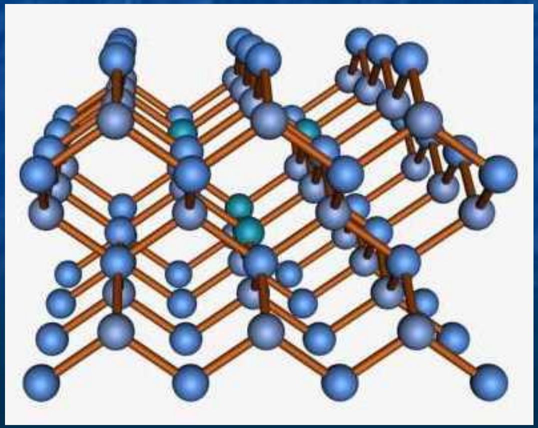
It is incredibly hard and strong!

	Knoop Hardness Index (kg/mm2)
Diamond	7000
Silicon Carbide	2480
Silicon	1150
Stainless Steel	600
Tungsten	485

So, large but thin wafers will not break with handling!

Strong bonds also → High thermal conductivity (carries away dissipated power)

And provides for almost flawless crystals (more about this later):



Step 2) Spray on or grow on additional layer

Alternative i) Spray via evaporation:

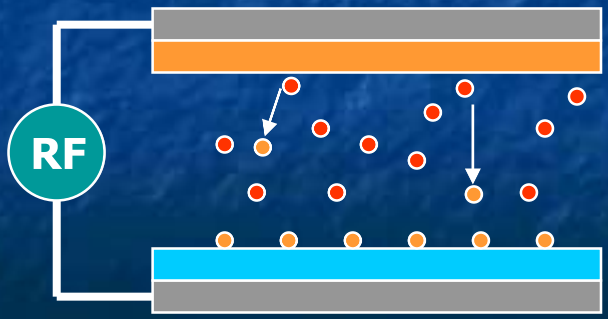
Heat up the material you want to deposit until it starts to fall apart

Do this in a vacuum so that what comes off goes in straight line and doesn't react with anything in-flight

However doesn't work for many materials that don't come apart as compounds

Example SiO_2 (solid) → SiO (vapor) + 1/2 O_2

Alternative ii) Spray via blasting (or "sputtering") - This DOES work with compounds!



Gas is excited, ionized and energized by RF field

It blasts desired material off one plate

To condense on other plate (covered with wafer)

Alternative iii) "Grow" a layer of what you want

Sort of like rusting iron: $2\ Fe + 3/2\ O_2 \rightarrow Fe_2O_3$

Except that where iron oxide is a crumbly porous mess,

Silicon oxide is . . . glass! Si (solid) + $1/2\ O_2$ (gas) $\rightarrow SiO_2$

Chemically, glass in incredibly tough

In what do chemists use to store almost ALL of their chemicals?

(Can almost count exceptions on one hand: HF, KOH . . .)

Although brittle, it is mechanically strong: *"fiber-glass" reinforced . . ."*

Can also "Grow" via gas phase chemical reactions:

$SiH_4 + O_2 \rightarrow SiO_2$ (solid) + $2\ H_2$ (Disclaimer: Goes "boom" if don't carefully dilute!!)

And works for other related insulators

$3\ SiH_4 + 4\ NH_4 \rightarrow Si_3N_4$ (solid) + $14\ H_2$

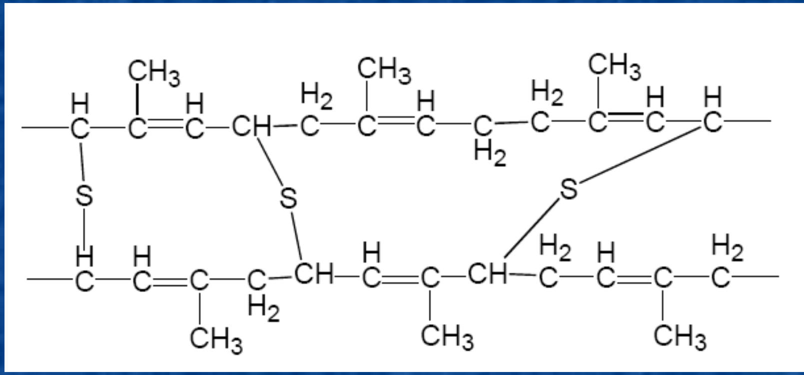
Step 3) Apply, expose, develop pattern in photographic emulsion

Emulsion is also called "resist" because we want it to resist chemical etching

OK, after glass, what is chemist's second choice for chemical container?

(HINT: Advice given to Dustin Hoffman's character in movie The Graduate -1967)

A "cross-linked" polymer (here "vulcanized" rubber)



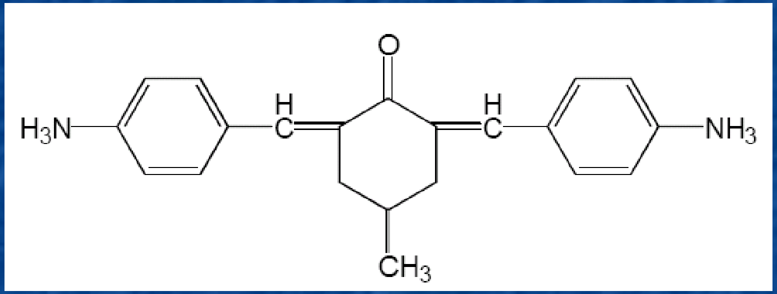
Hydrocarbon monomers (lone carbon-based chains) can be very chemically resistant

Are here held together by the sulfur atoms - But sulfur linking is induced by heat not light!!

So you need different LIGHT stimulated way of linking/unlinking monomers

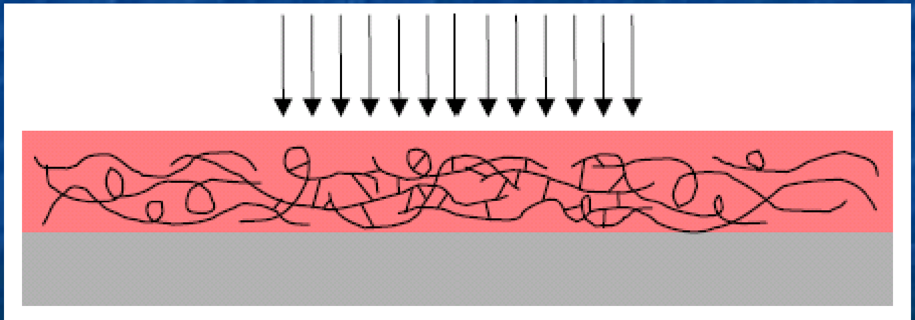
One way (used in Kodak's KTFR, workhorse of the early integrated circuits):

2,6-bis(4-azidobenzal)-4-methylcyclohexanone or just "ABC" (I didn't make this up!)



Light reacts with "azide" NH_3 end units, converting them to reactive radicals

So that they then bind themselves to the monomers ("cross-linking" them):



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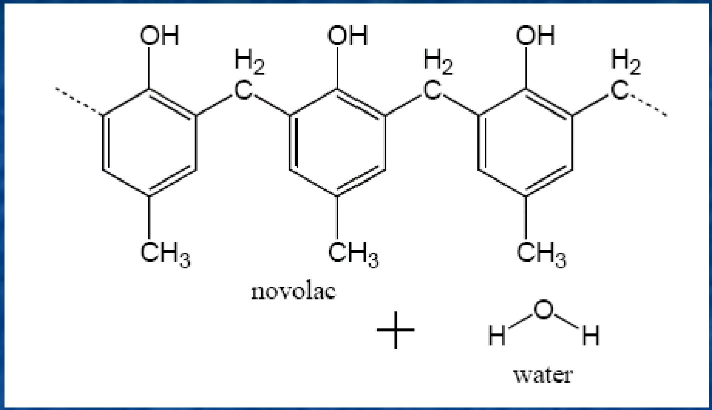
Modern "photoresists" use different chemical mixtures and different tricks:

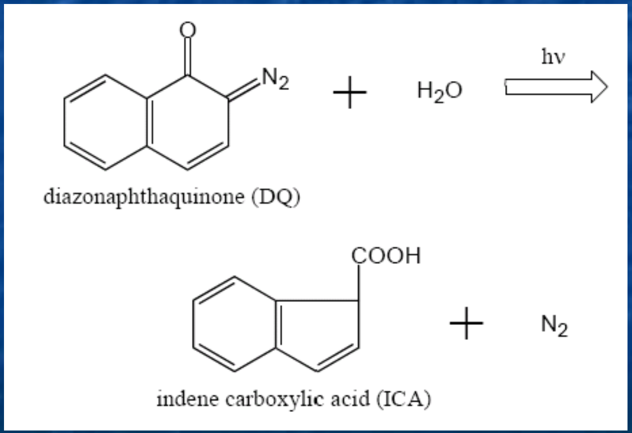
Phenolic "resin" (monomer):



Source: R. Bruce Darling
University of Washington

PLUS photoactive compound (PAC) that light switches from hydrophobic to philic

Where not struck by light →
Sheds water-based remover
(and thus everything stays put)

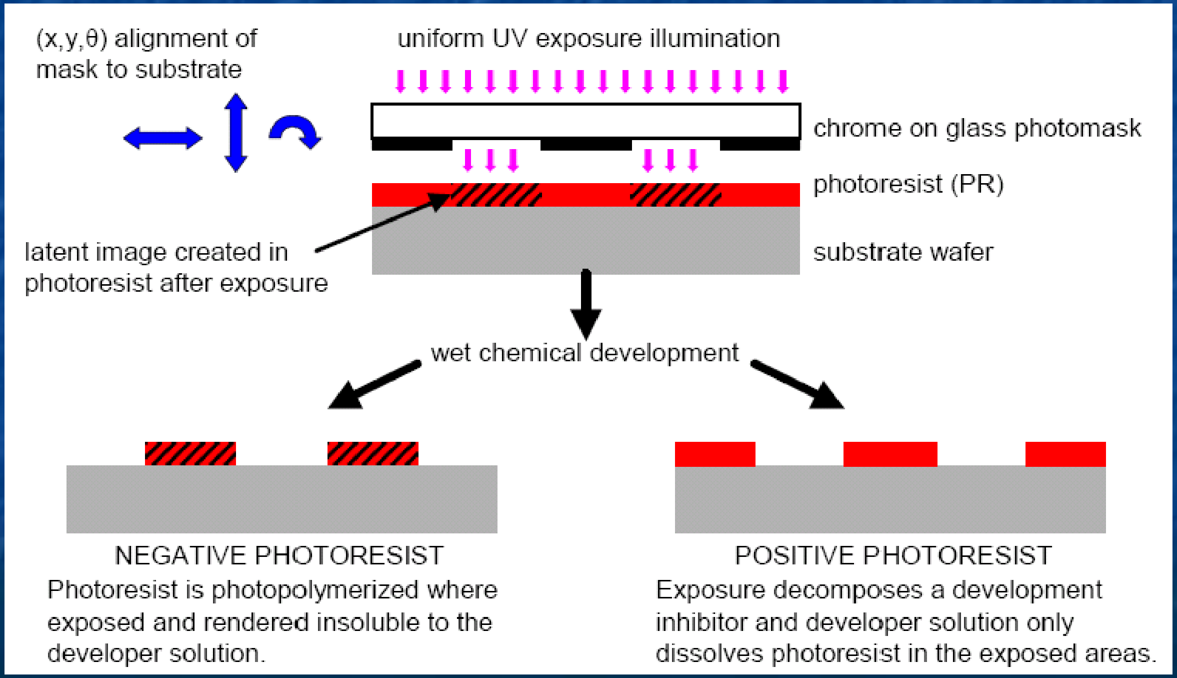


Where hit by light, sucks in
water-based remover
(which removes all)

Apply this "resist" to the wafer by spinning it on:

Source: R. Bruce Darling
University of Washington

Then expose pattern through photographic shadow "mask:"



Source: R. Bruce Darling
University of Washington

Actually done in a tool called a "mask aligner" which (in older non-automated versions):

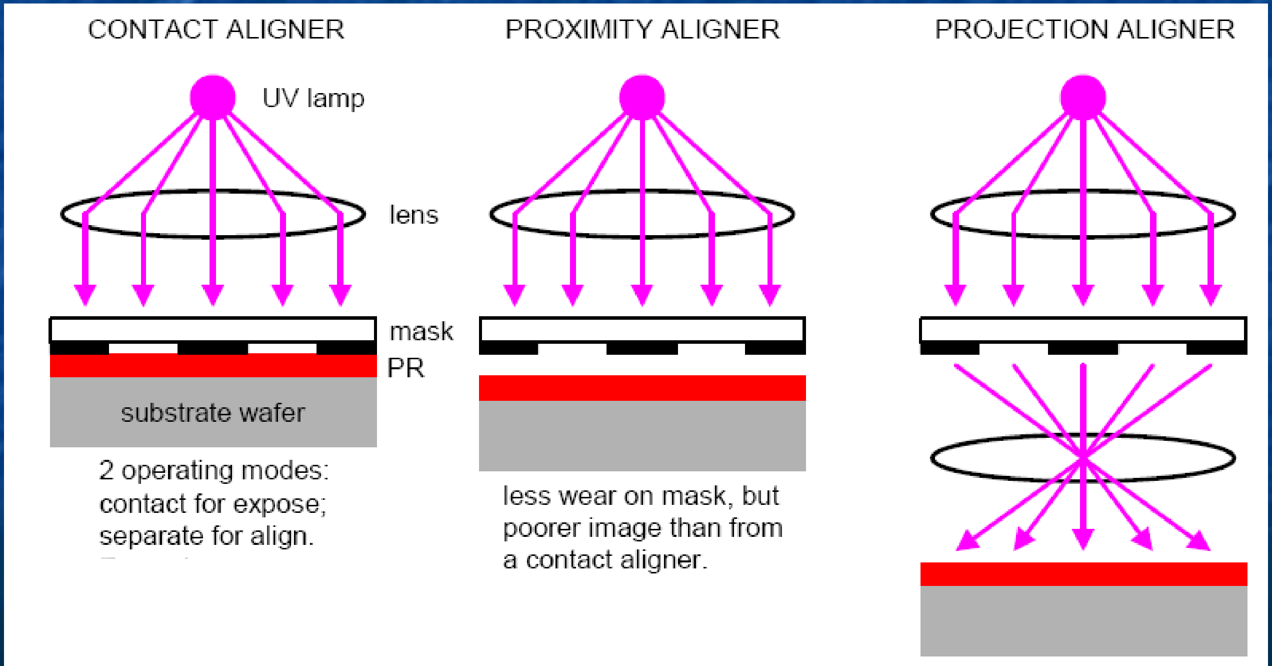
- Uses microscope allowing you to first position the resist covered wafer below the mask

- In "contact" machine, it then clamps resist/wafer tightly against mask

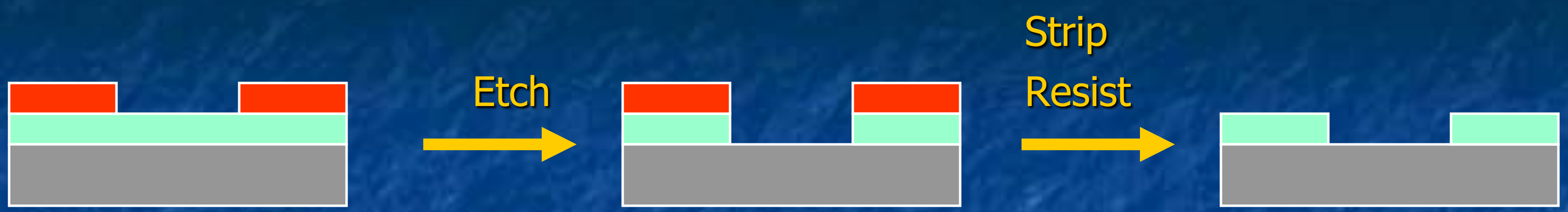
- UV light is then projected down through transparent regions of mask onto resist/wafer

In "projection" machine, shadow image of mask is de-magnified and projected onto resist/wafer at perhaps 1/5 original mask size.

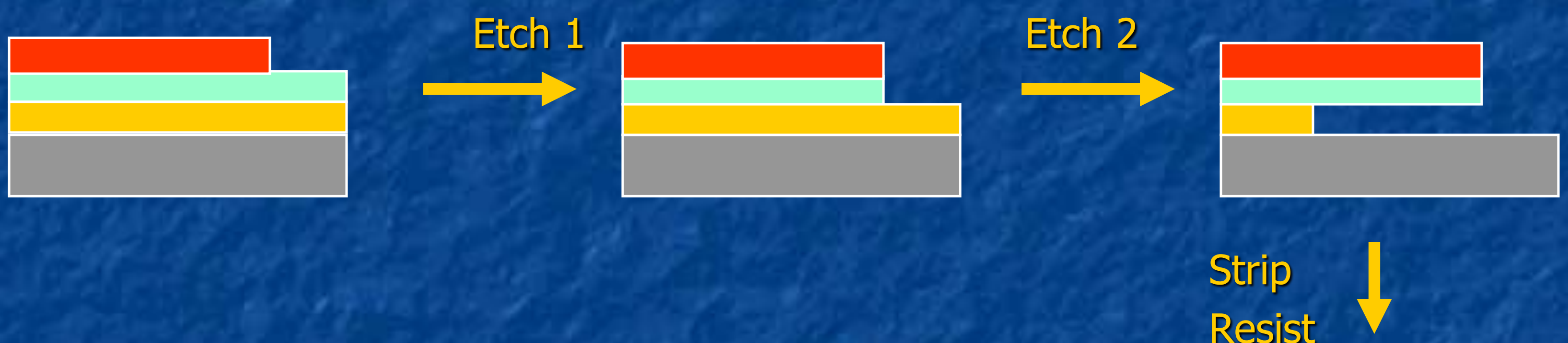
- Wafer is then released, "stepped" to new position, and a new area exposed



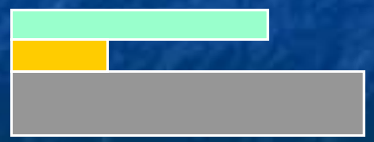
Step 4) Etch or blast away material not protected by emulsion



But can also get fancy and use multiple layers and multiple etches:



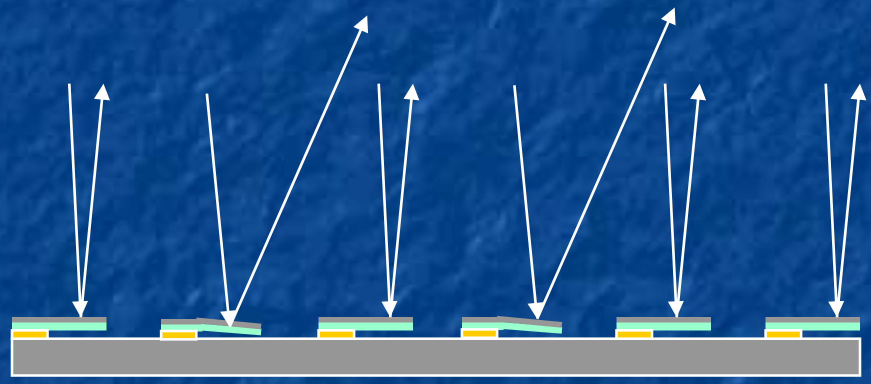
End up with a sort of diving board like structure:



What if "diving board" were metallic (or covered by metal)?

And you then applied suitable voltages:

And tried bouncing a laser off a whole bunch of these:



Remember: all "diving boards" made SIMULTANEOUSLY

What would you get? *Hints: 1) I talked about this technology in lecture 1*

2) We MAY be using it at this very moment

It's the Heart of a "DLP" Projection TV

From the DLP.com / Texas Instruments Website:

Voltage applied at front

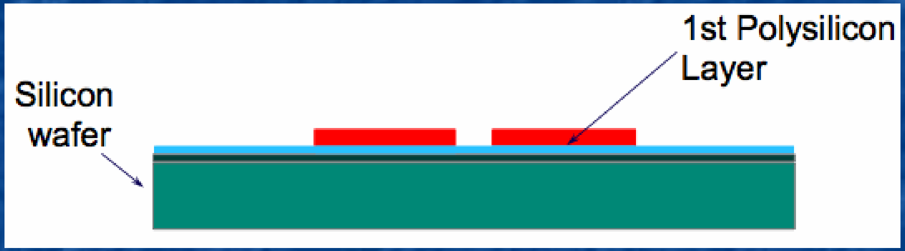
Voltage applied at rear:

But how did they make those bound yet free-to-rotate gears?

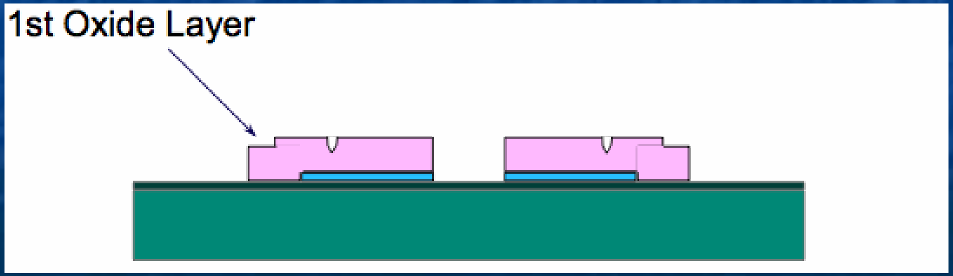
Couldn't get an answer from Sandia, but did find this in another prof's lecture notes:

Source: Prof. LaVern Starman, Wright State University
http://www.cs.wright.edu/people/faculty/kxue/mems/MEMS_3FabricationM06.pdf

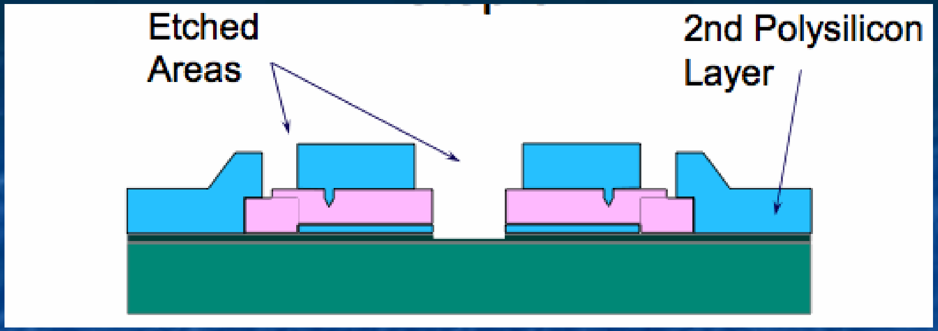
On a substrate (likely a Si wafer with capping layers) deposit layer of polycrystalline Si (baby blue). Then deposit and pattern a photoresist layer (red):



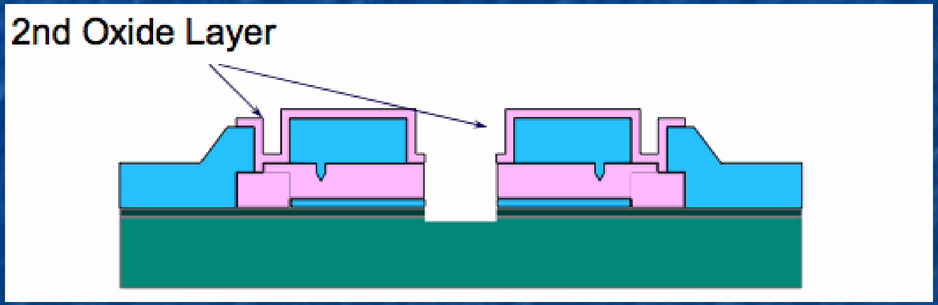
Deposit and pattern a thick oxide layer (pale purple):



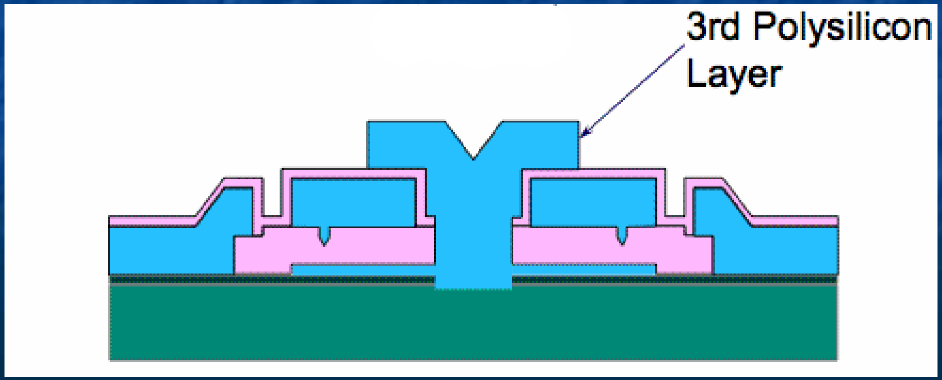
Deposit and pattern a second polysilicon layer (pale blue):



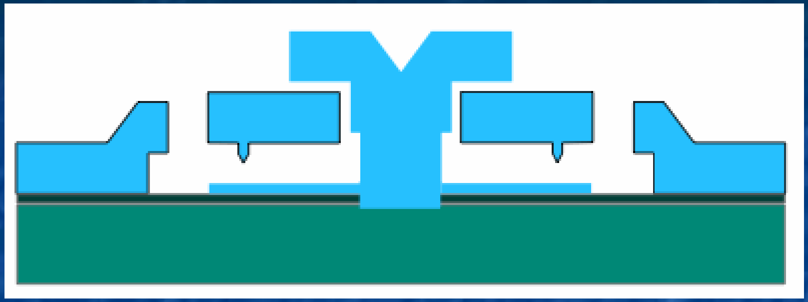
Deposit and pattern a thin oxide layer (pale purple):



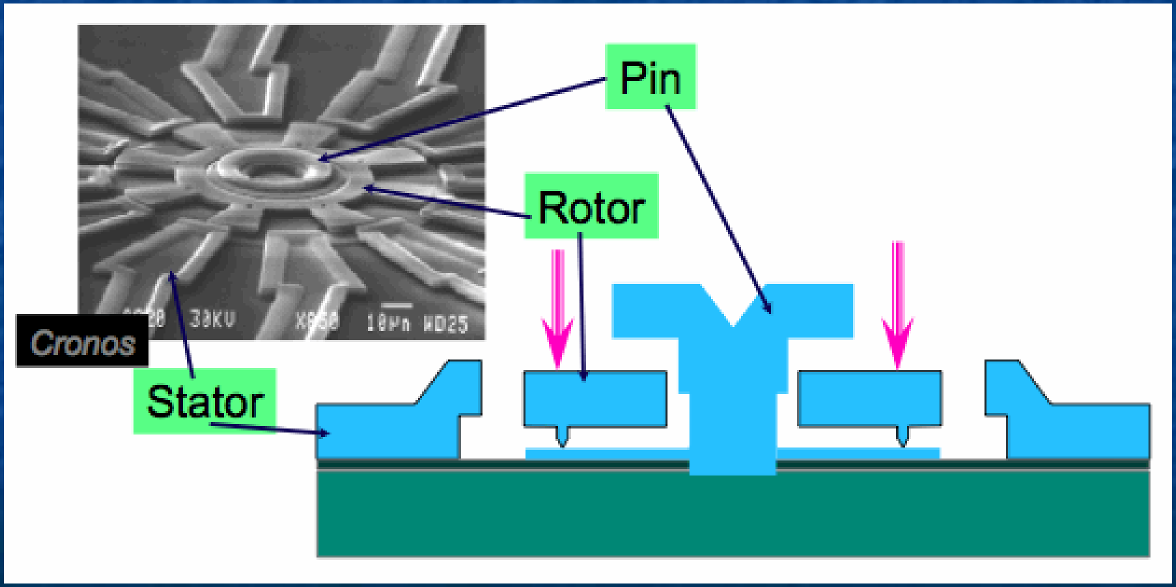
Deposit and pattern a third polysilicon layer (pale blue):



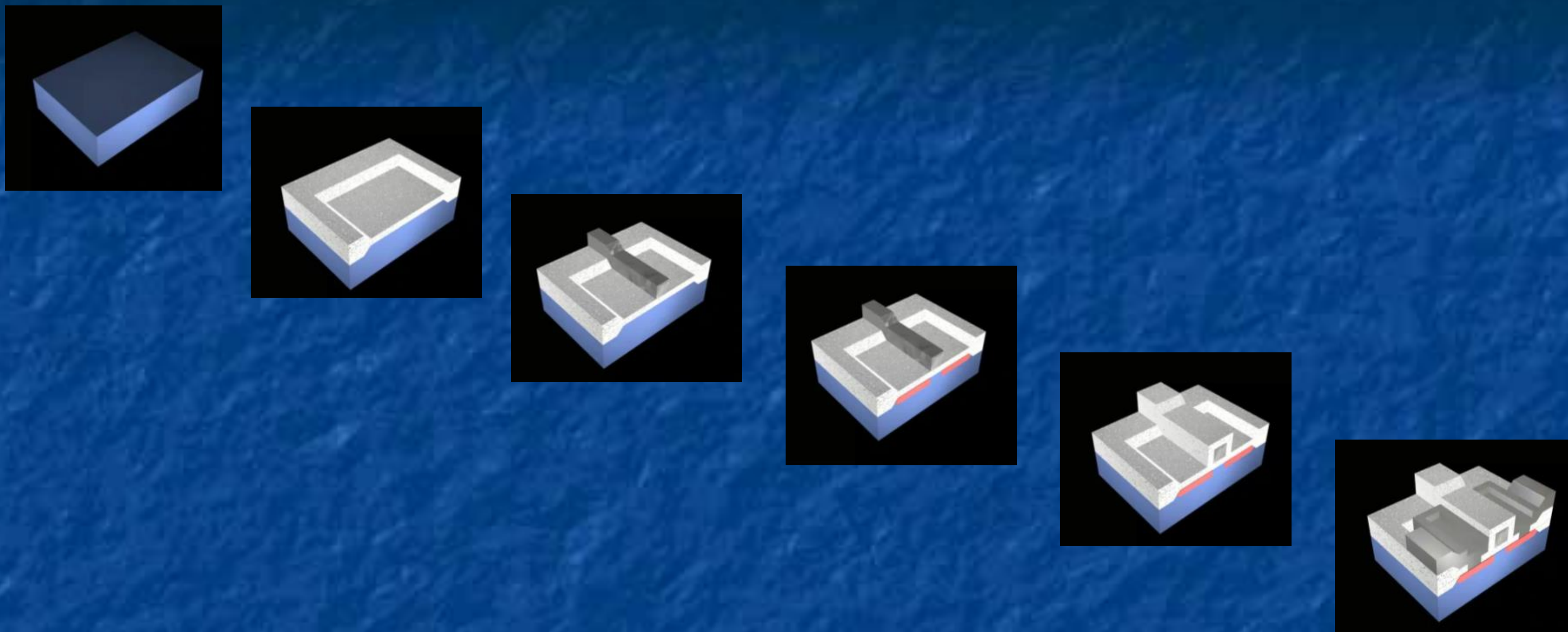
Etch away "sacrificial" oxide layers using hydrofluoric (HF) acid:



Rotating ring then settles onto base yielding final structure of MEMS electric motor:



Or can use to make the transistors of an integrated circuit:



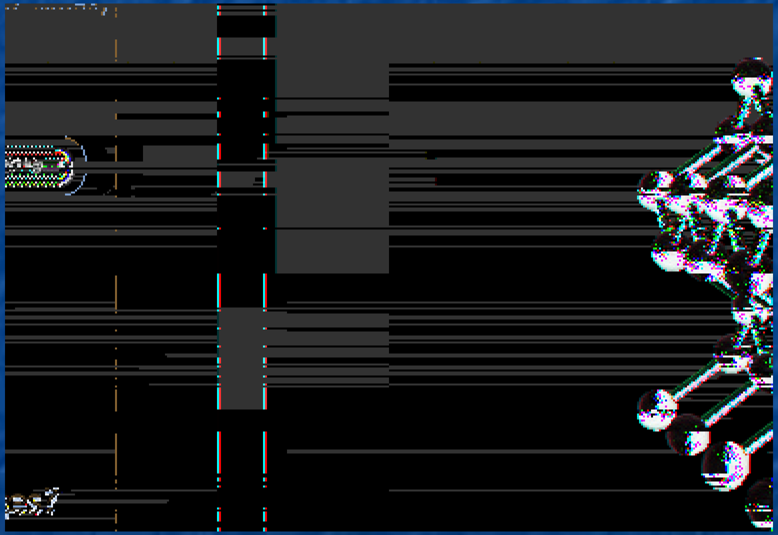
To complete Microfabrication's bag of tricks, need one more thing:

"Anisotropic Etching"

By default, etches (liquid or gas) tend to etch at ~ same rate in any direction

But, Crystals + Very Special Etches → Direction dependent (anisotropic) etching

Depends on exact form of atoms at crystal's (e.g. silicon) surface:



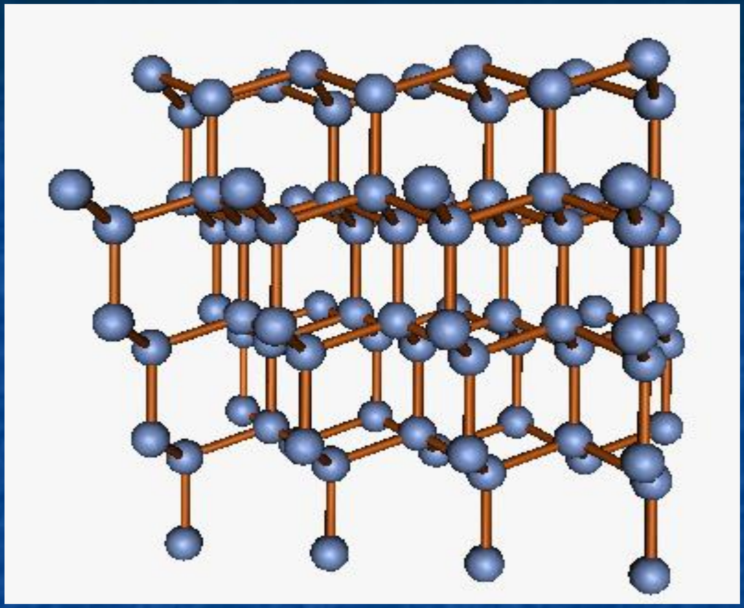
Look closely at the top surface of this Si crystal

EVERY atom on this top plane has TWO bonds to TWO atoms in plane below

As EVERY atom in second plane is also bonded with two bonds to two atoms below it

This surface is called a (100) crystal surface

Compare to different face of SAME (Si) crystal:



EVERY atom in topmost plane has THREE bonds to THREE atoms in plane below

EVERY atom in next plane has ONE bond to ONE atom in plane below it

This surface is called a "(111)" crystal surface

To remove atom from surface of PREVIOUS crystal, must always break 2 bonds

To remove atom from surface of THIS crystal, alternate breaking 3 bonds then 1

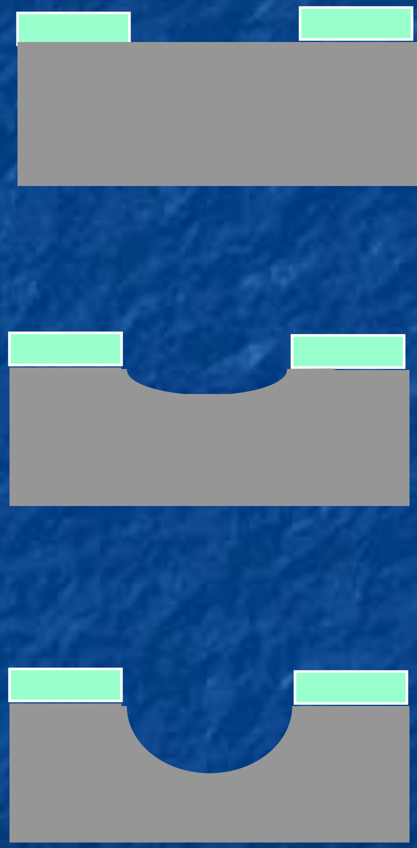
1 bond = easy to break

2 bonds = harder to break

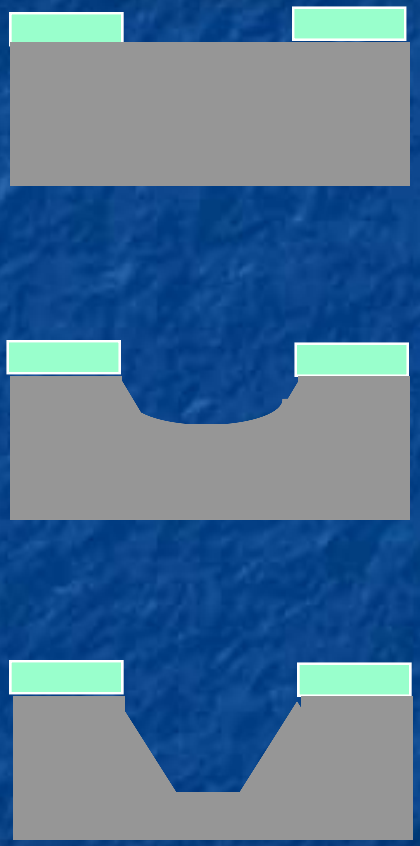
3 bond = very hard to break *Etch can come to a complete stop on "(111)" !!!*

Normal vs. Anisotropic Etch:

Normal (isotropic):

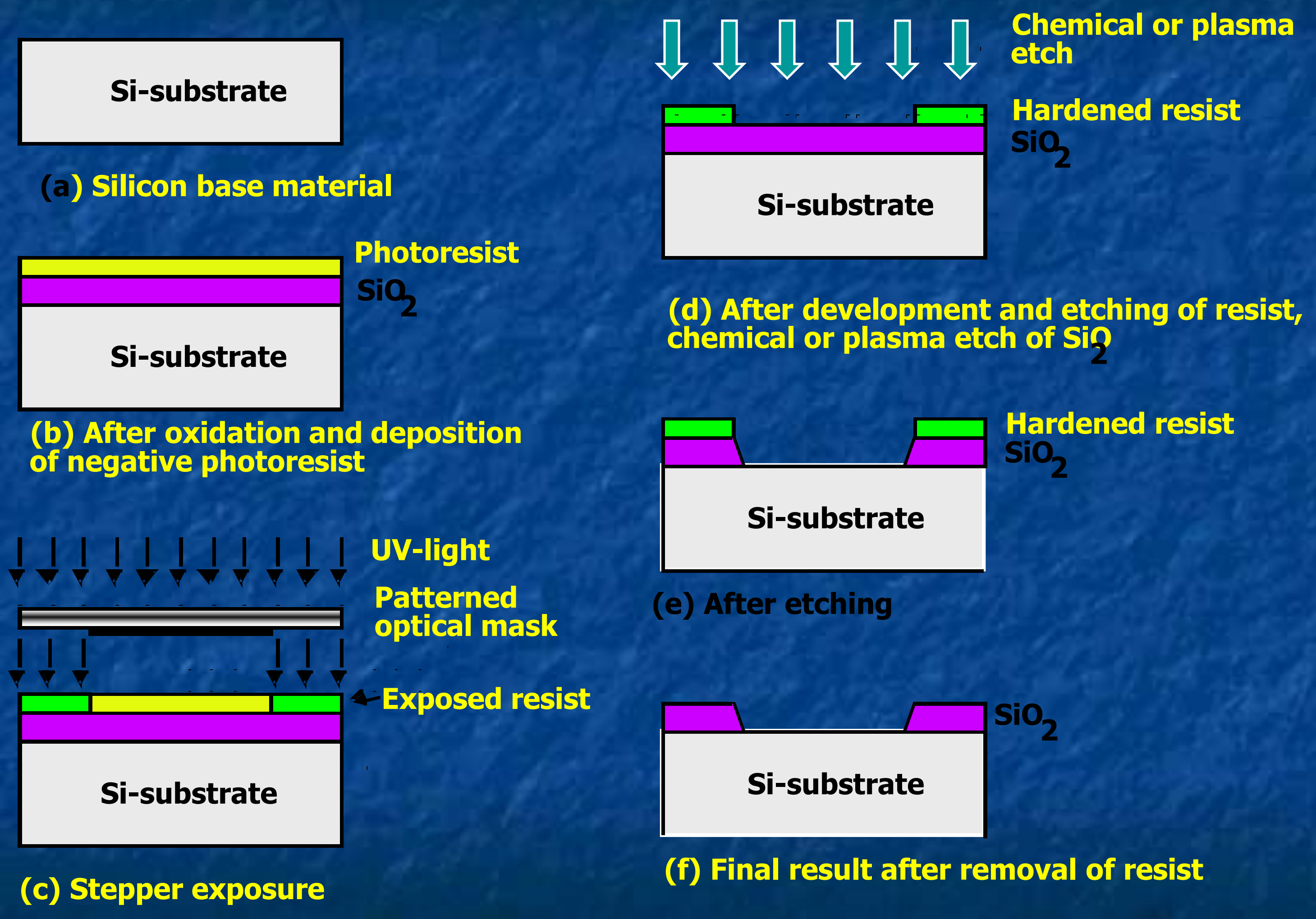


Anisotropic:



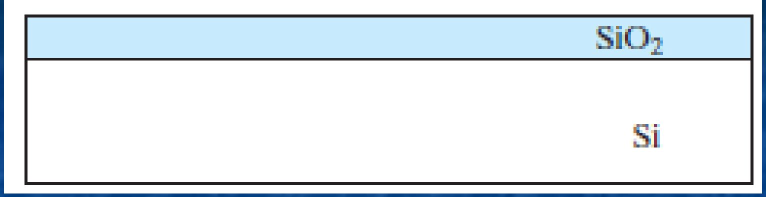
Anisotropic etched surface develops (111) facets !!!

Patterning of SiO2

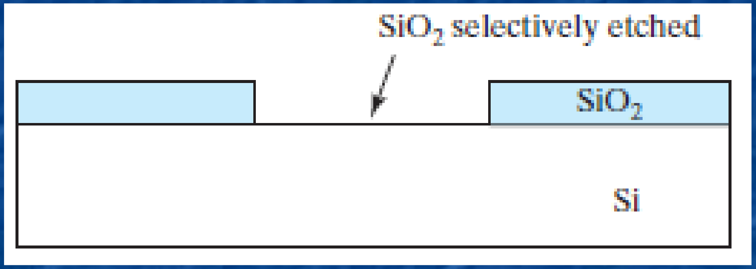


Introduction to Device Fabrication

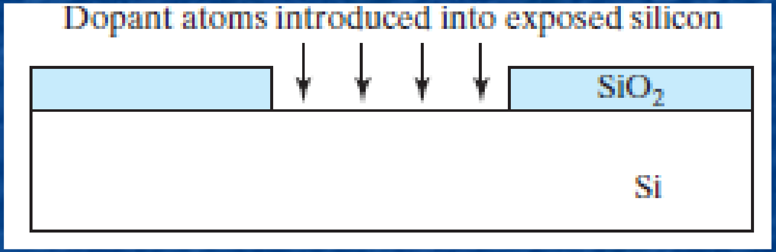
Oxidation



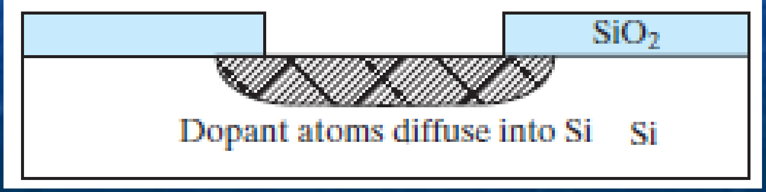
Lithography & Etching



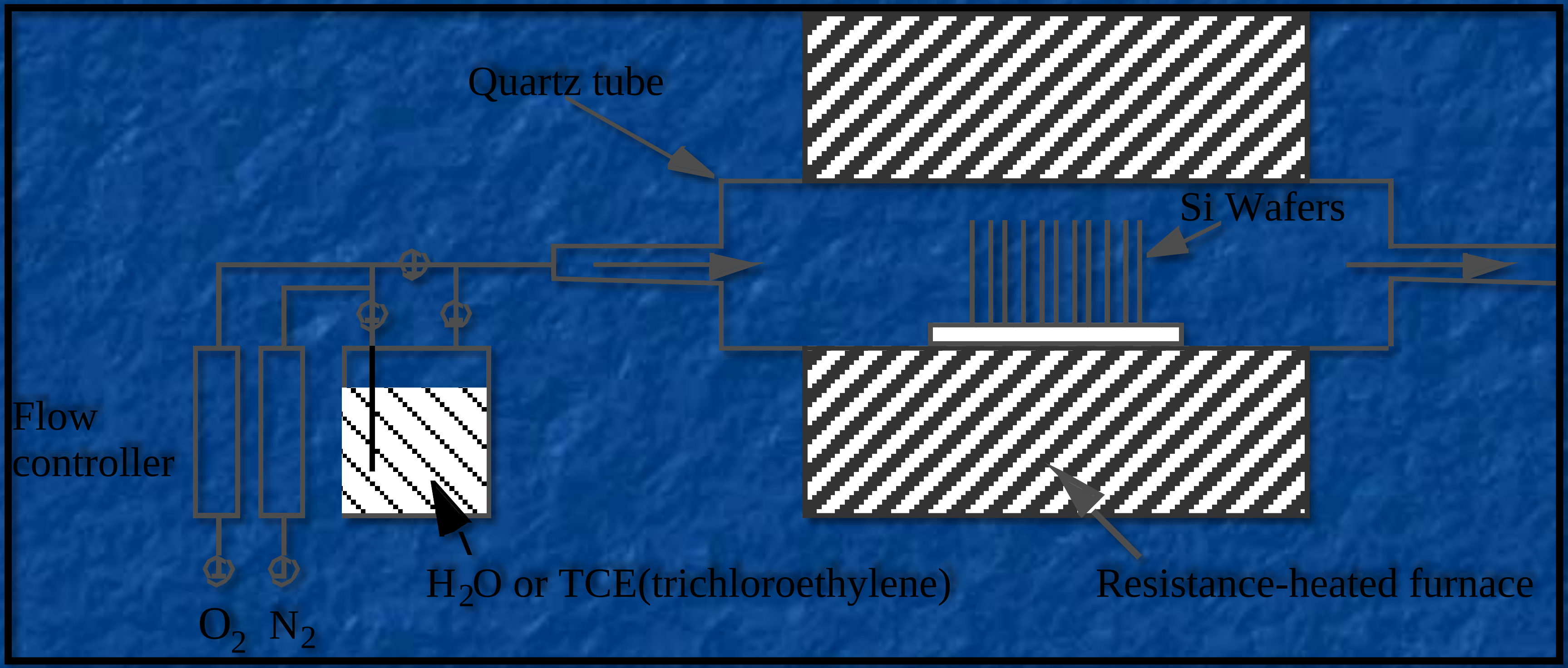
Ion Implantation



Annealing & Diffusion



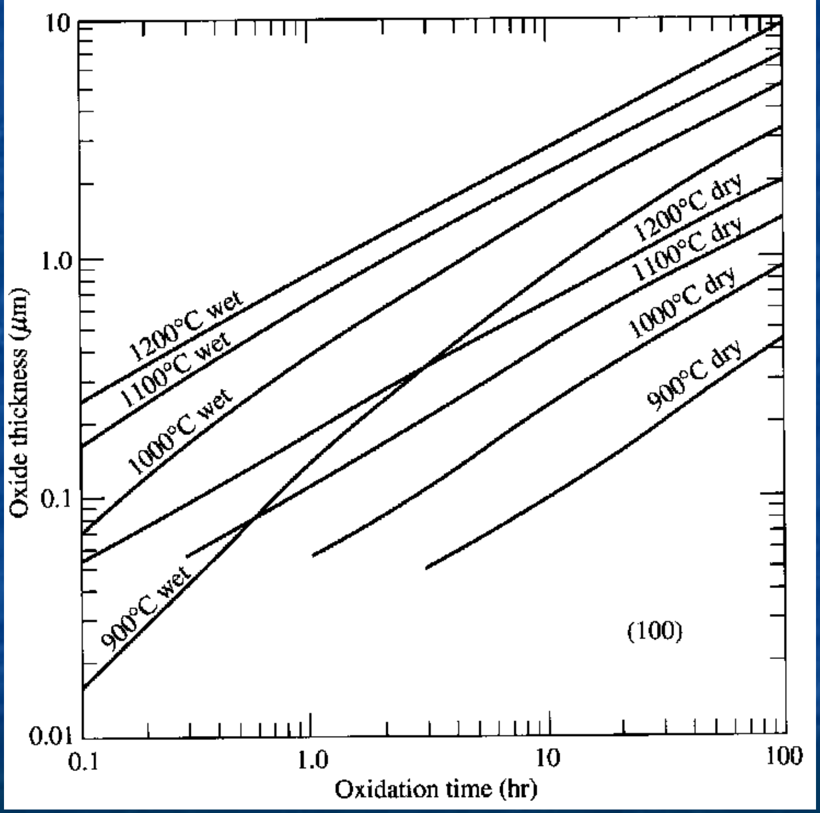
Oxidation of Silicon



Oxidation of Silicon

Dry Oxidation : $Si + O_2 \rightarrow SiO_2$

Wet Oxidation : $Si + 2H_2O \rightarrow SiO_2 + 2H_2$



Oxidation of Silicon

EXAMPLE : Two-step Oxidation

(a) How long does it take to grow 0.1μm of dry oxide at 1000 °C ?

(b) After step (a), how long will it take to grow an additional 0.2μm of oxide at 900 °C in a wet ambient ?

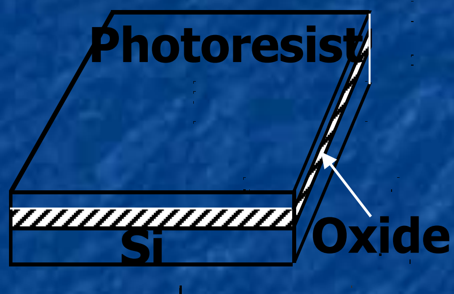
Solution:

(a) From the "1000°C dry" curve in previous Slide , it takes 2.5 hr to grow 0.1μm of oxide.

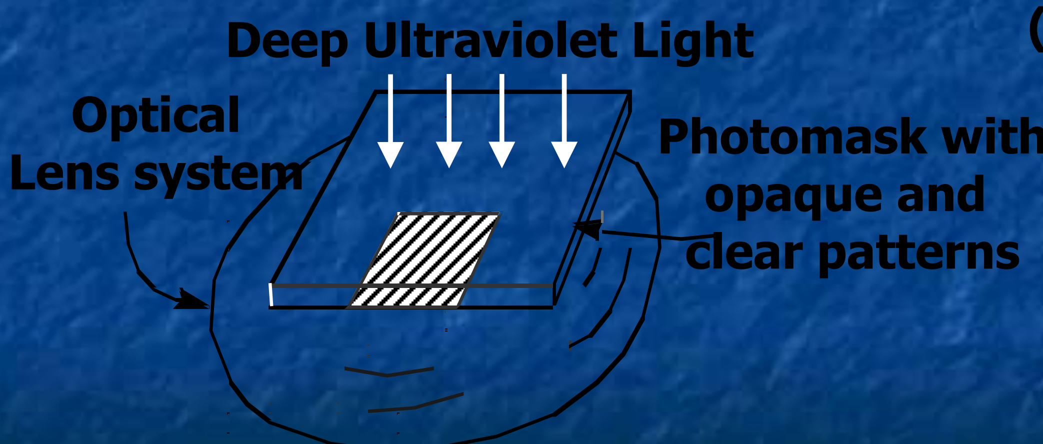
(b) Use the "900°C wet" curve only. It would have taken 0.7hr to grow the 0.1 μm oxide and 2.4hr to grow 0.3 μm oxide from bare silicon. The answer is 2.4hr–0.7hr = 1.7hr.

Lithography

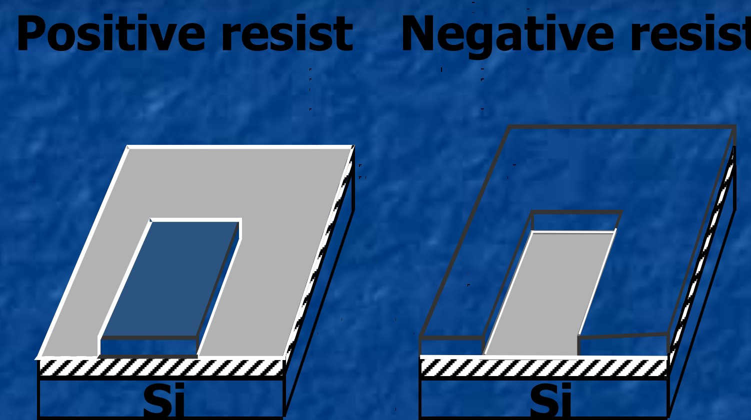
(a) Resist Coating



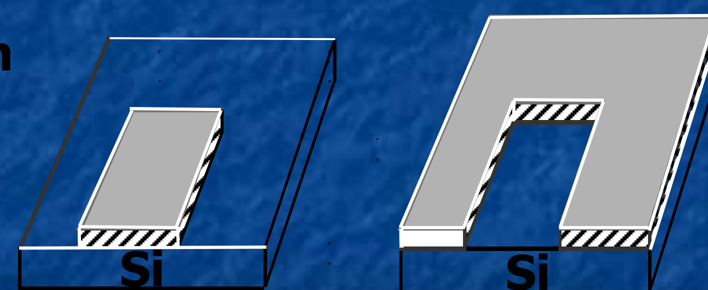
(b) Exposure



(c) Development



(d) Etching and Resist Strip



Lithography

Photolithography Resolution Limit, *R*

• $R \geq k\lambda$ due to optical diffraction

• Wavelength λ needs to be minimized. (248 nm, 193 nm, 157 nm?)

• k (<1) can be reduced will

• Large aperture, high quality lens

• Small exposure field, step-and-repeat using "stepper"

• Optical proximity correction

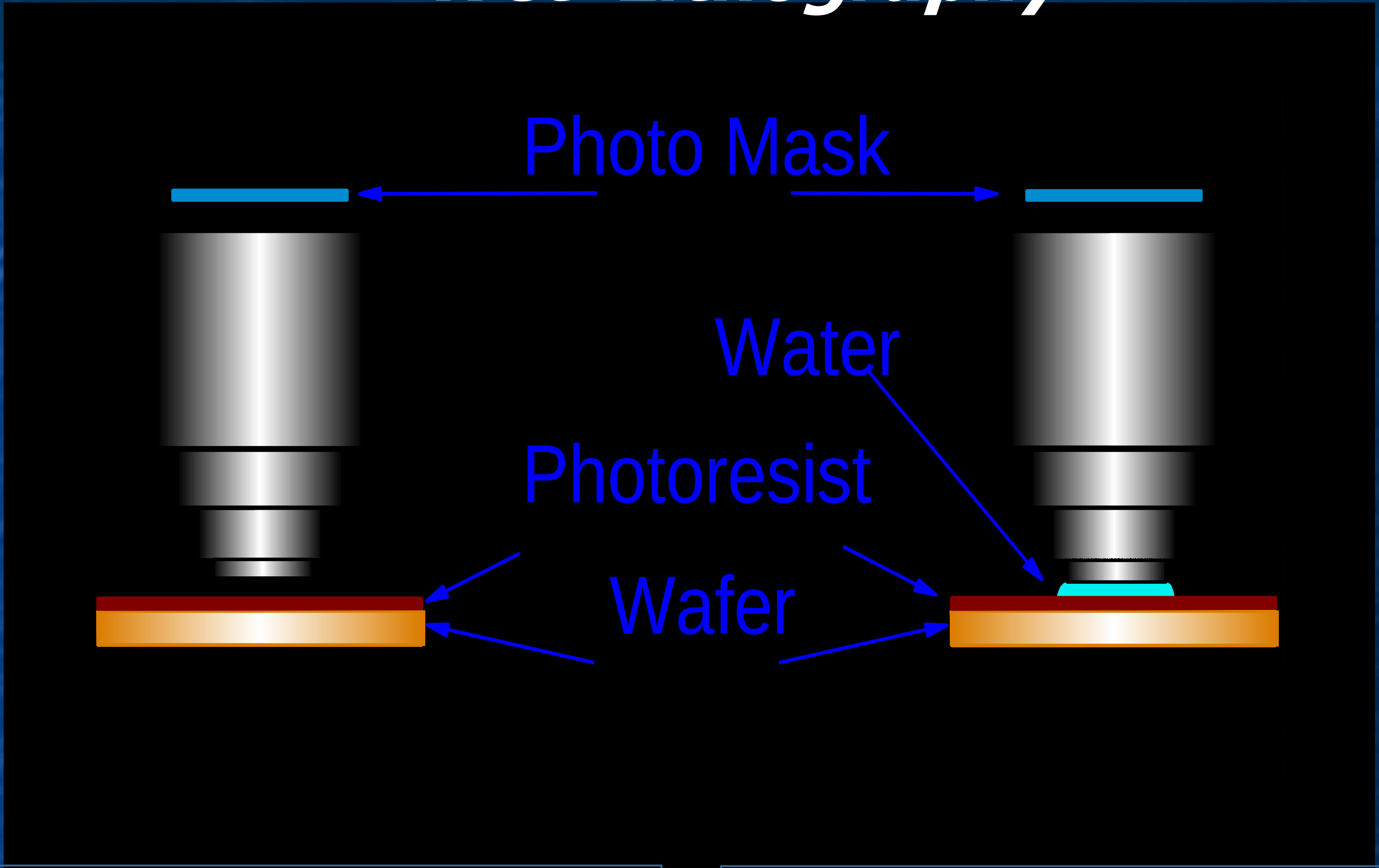
• Phase-shift mask, etc.

• Lithography is difficult and expensive. There can be 40 lithography steps in an IC process.

Lithography

Wafers are being loaded into a stepper in a clean room.

Wet Lithography

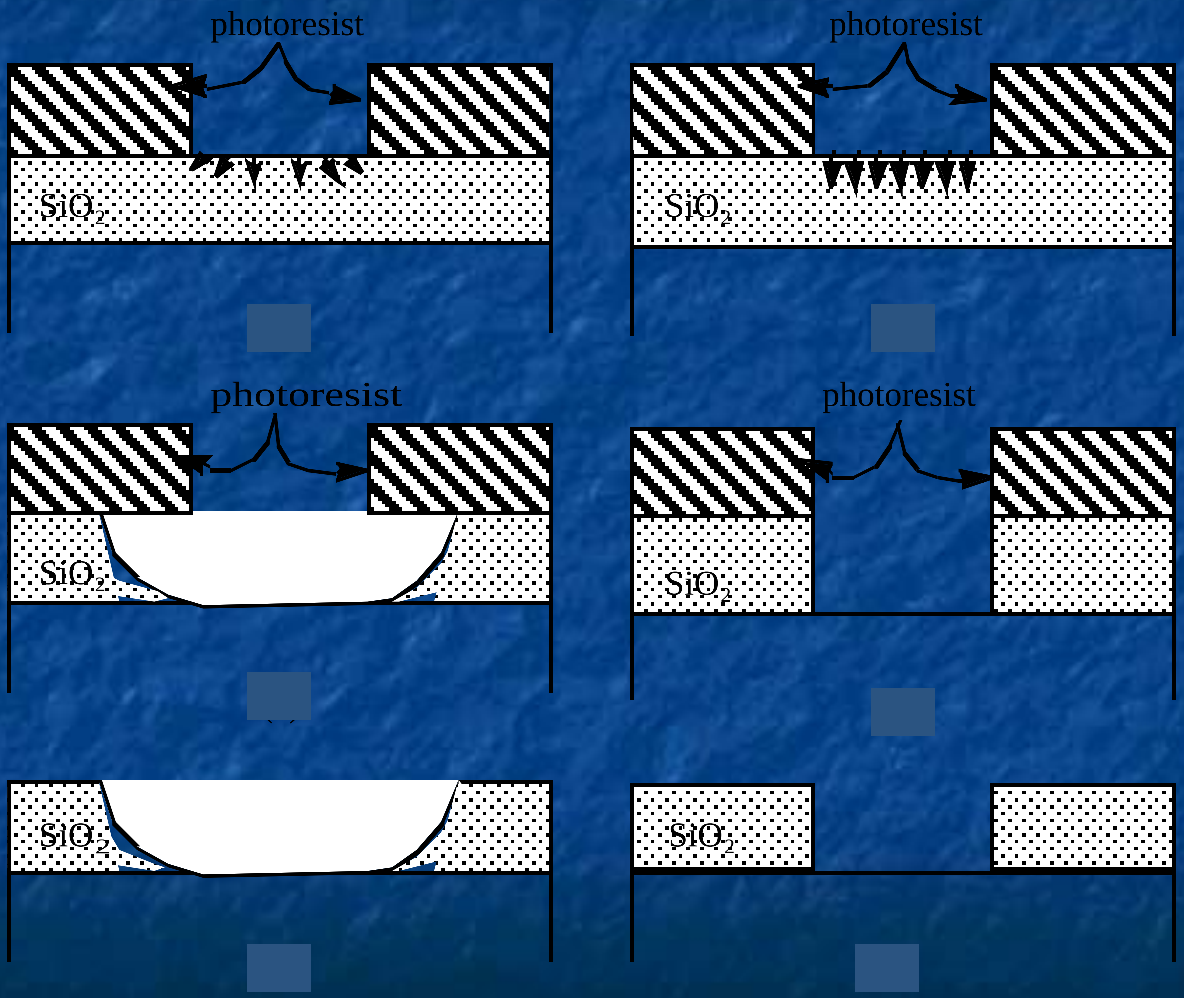


conventional dry lithography

wet or immersion lithography

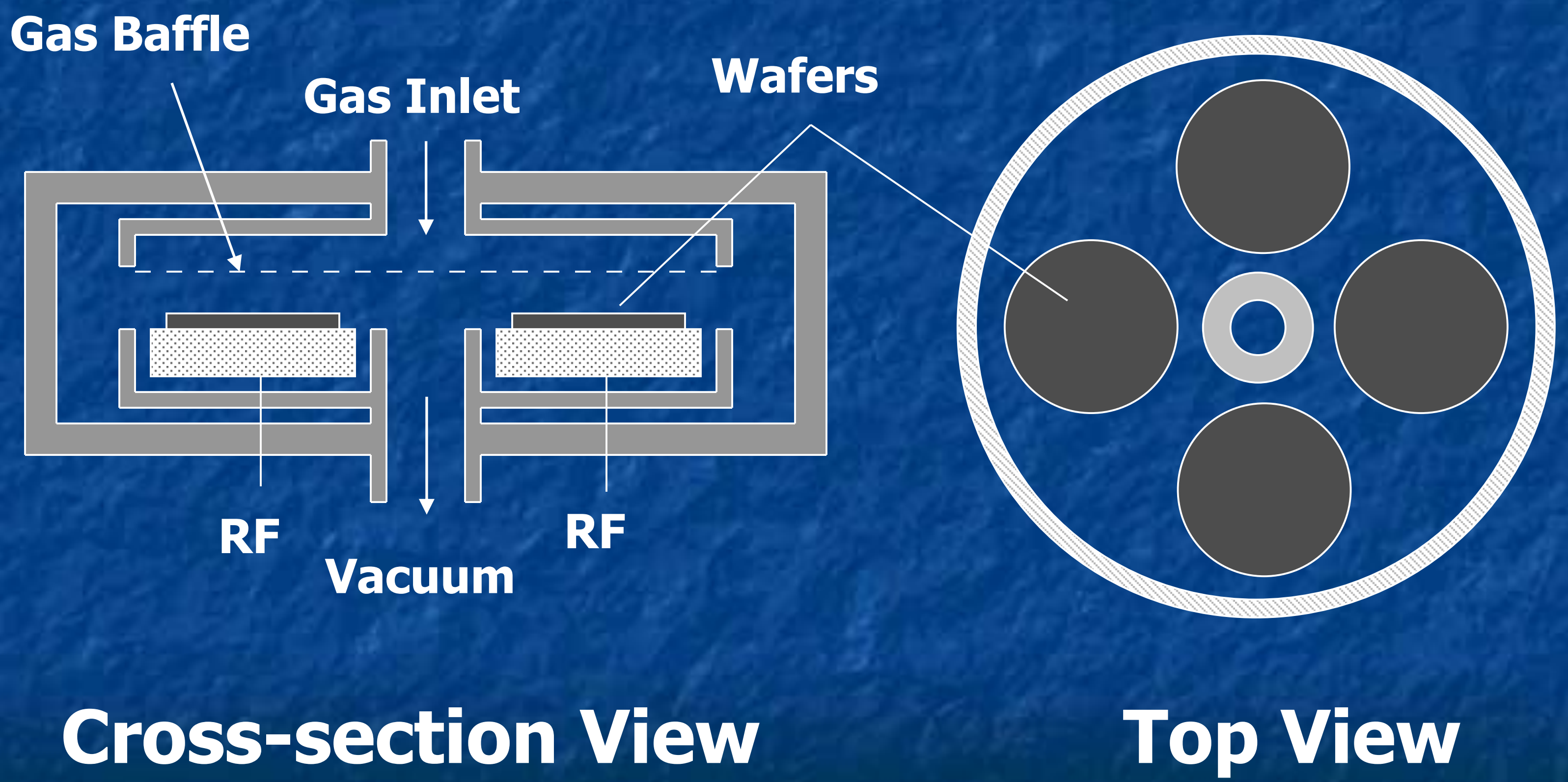
Pattern Transfer–Etching

Isotropic etching / Anisotropic etching



Pattern Transfer–Etching

Reactive-Ion Etching Systems



Pattern Transfer–Etching

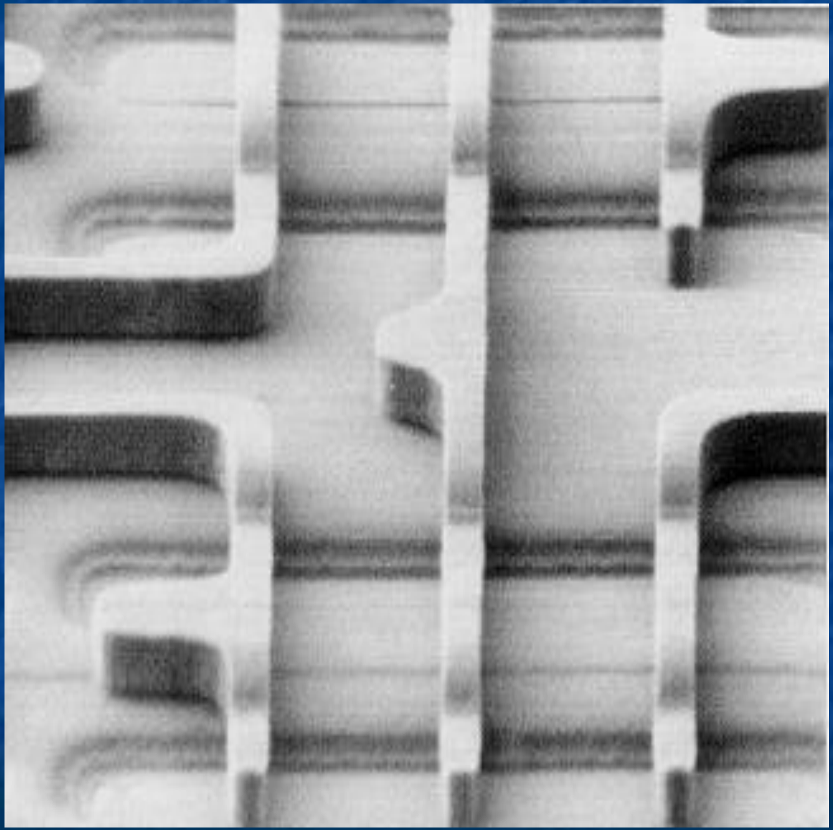
Dry Etching (also known as Plasma Etching, or Reactive-Ion Etching) **is anisotropic.**

- **Silicon and its compounds can be etched by plasmas containing F.**
- **Aluminum can be etched by Cl.**
- **Some concerns :**

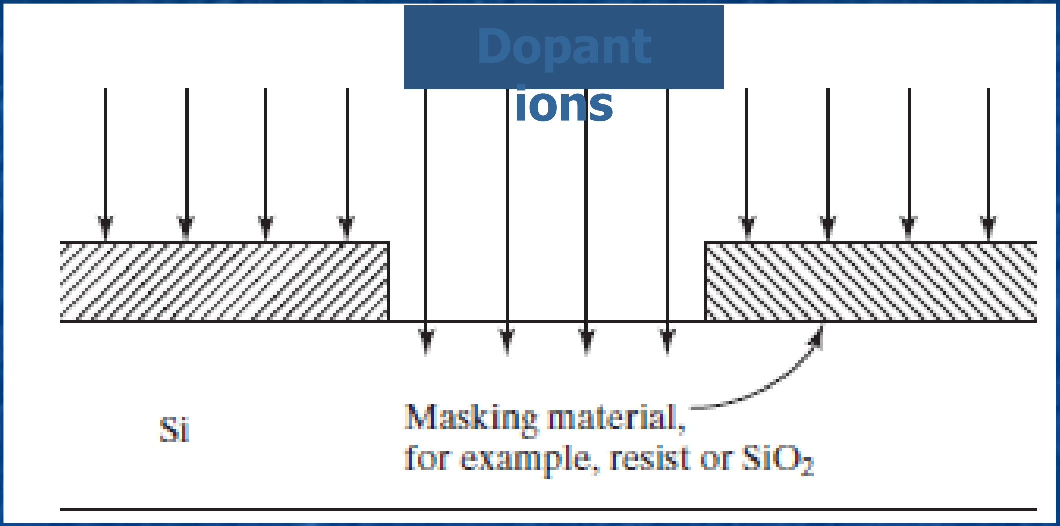
- Selectivity and End-Point Detection

- Plasma Process-Induced Damage or Wafer Charging Damage and Antenna Effect

Scanning electron microscope view of a plasma-etched 0.16 μm pattern in polycrystalline silicon film.



Doping
Ion Implantation



- The dominant doping method
- Excellent control of dose (cm^{-2})
- Good control of implant depth with energy (KeV to MeV)
- Repairing crystal damage and dopant activation requires annealing, which can cause dopant diffusion and loss of depth control.

Other Doping Methods

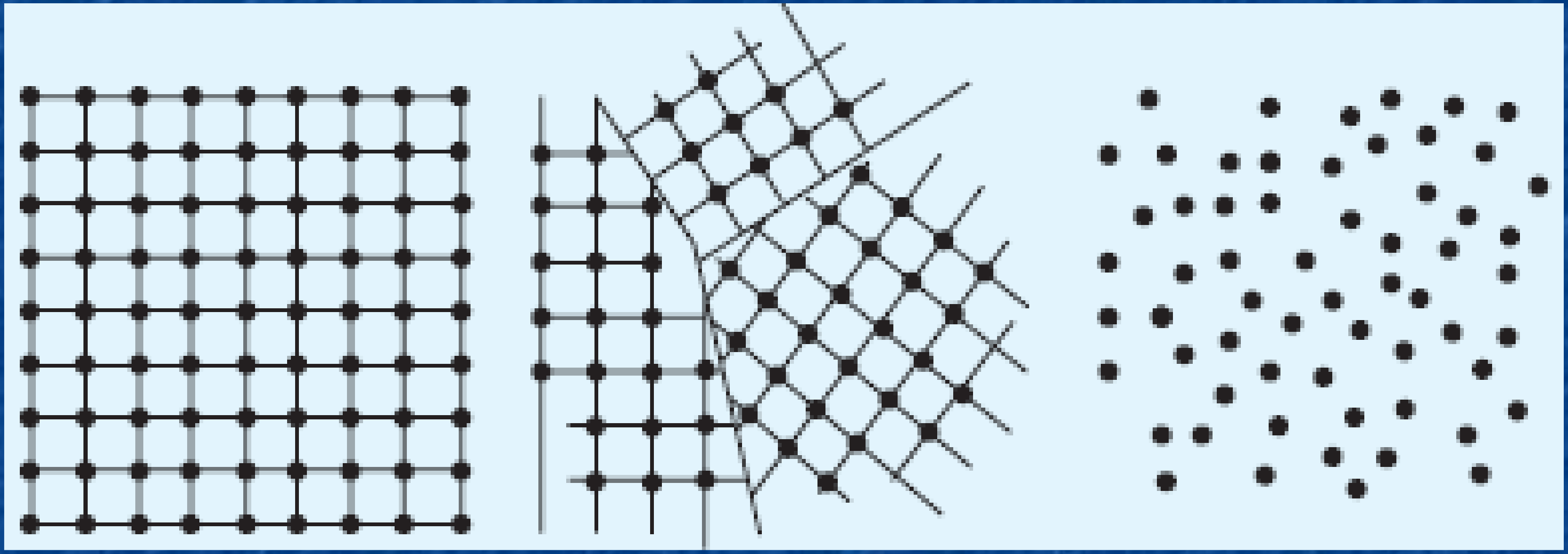
- ***Gas-Source Doping*** **: For example, dope Si with P using $POCl_3$.**

- ***Solid-Source Doping*** **: Dopant diffuses from a doped solid film (SiGe or oxide) into Si.**

- ***In-Situ Doping*** **: Dopant is introduced while a Si film is being deposited.**

Thin-Film Deposition
Three Kinds of Solid

Crystalline | **Polycrystalline** | **Amorphous**



Example: Silicon wafer

Thin film of Si or metal.

Thin film of SiO_2 or Si_3N_4.

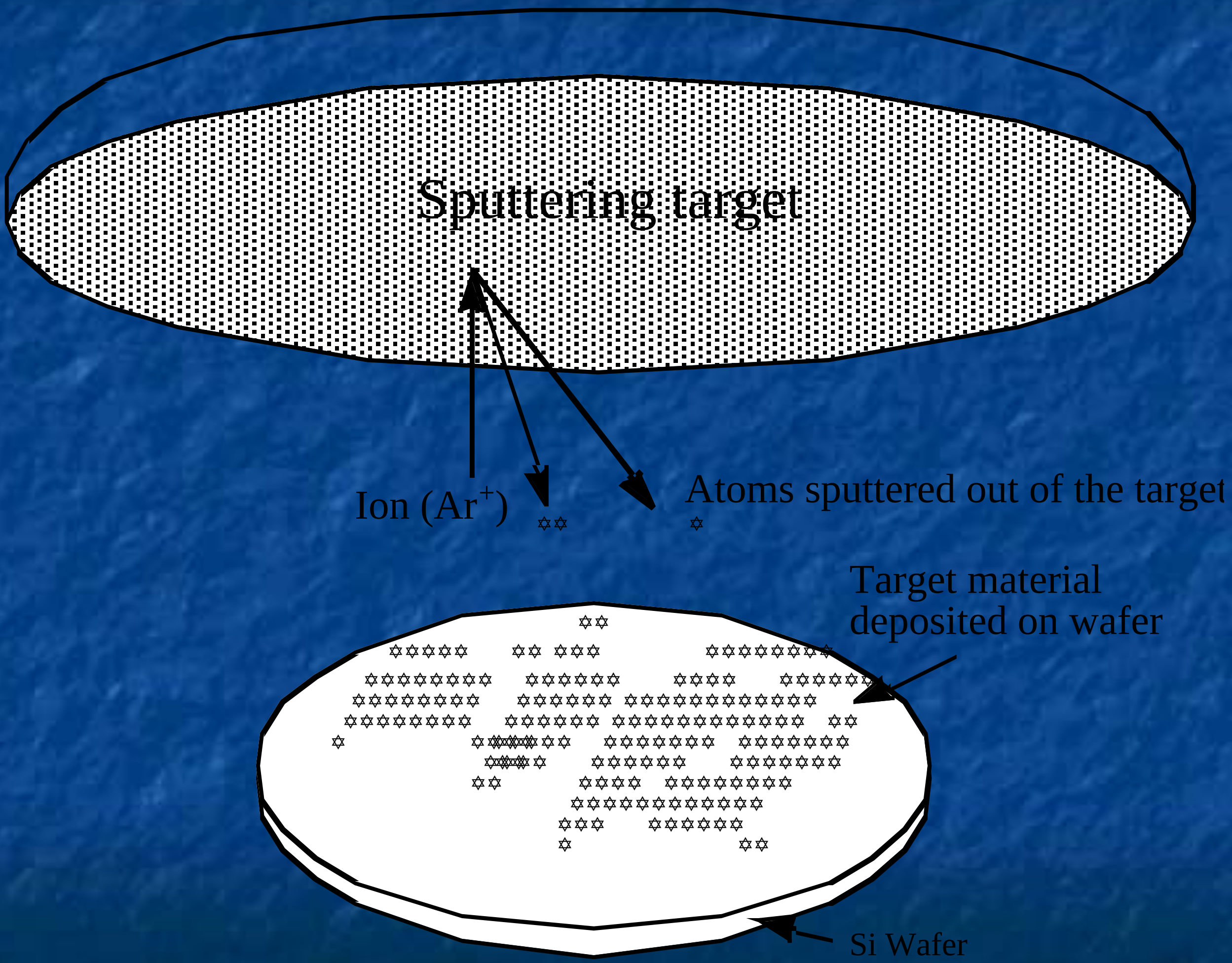
Thin-Film Deposition

Examples of thin films in integrated circuits

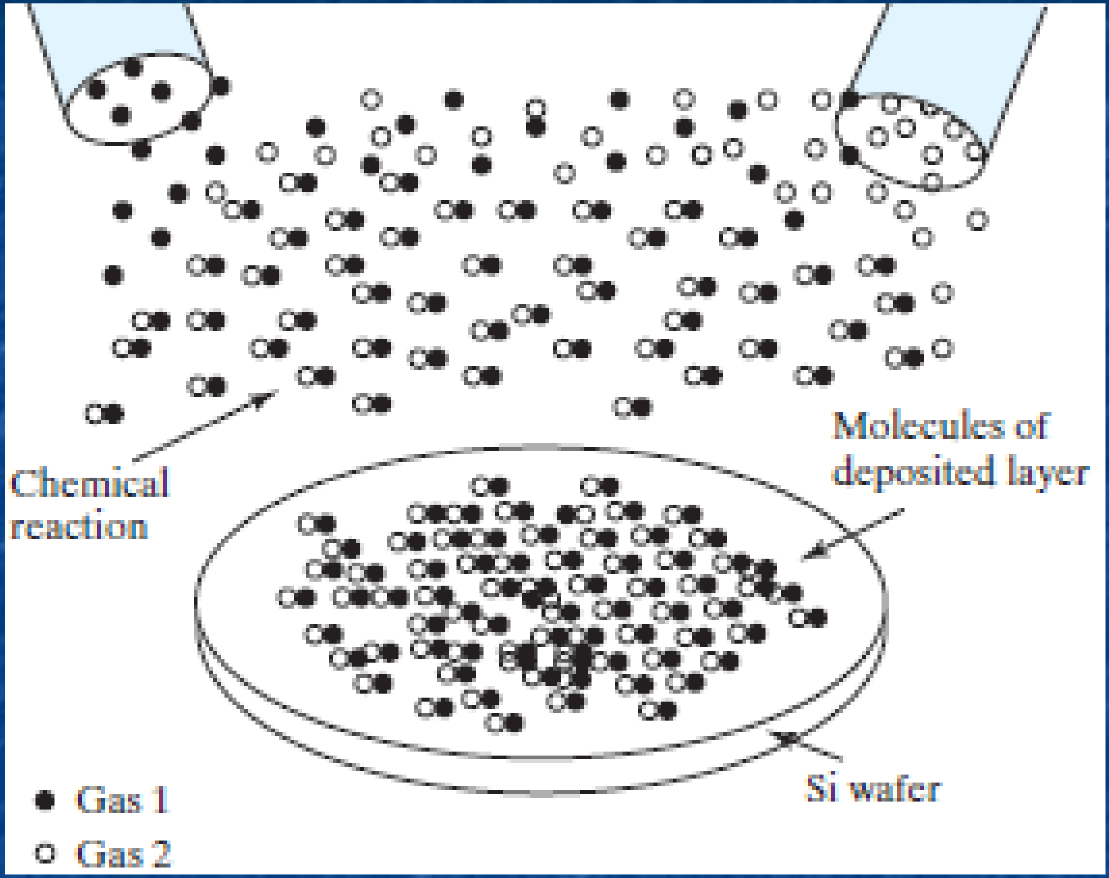
- Advanced MOSFET gate dielectric
- Poly-Si film for transistor gates
- Metal layers for interconnects
- Dielectric between metal layers
- Encapsulation of IC

Sputtering

Schematic Illustration of Sputtering Process



Chemical Vapor Deposition (CVD)



Thin film is formed from gas phase components.

Some Chemical Reactions of CVD

Poly-Si : SiH_4 (g) $\longrightarrow$ Si (s) + $2H_2$ (g)

Si3N4 : $3SiH_2Cl_2$ (g)+$4NH_3$ (g) $\longrightarrow$ Si_3N_4 (s)+6HCl(g)+$6H_2$ (g)

SiO2 : SiH_4 (g) + O_2 (g) $\longrightarrow$ SiO_2 (s) + $2H_2$ (g)

or

SiH_2Cl_2 (g)+$2N_2O$ (g) $\longrightarrow$ SiO_2 (s)+2HCl (g)+$2N_2$ (g)

Chemical Vapor Deposition (CVD)

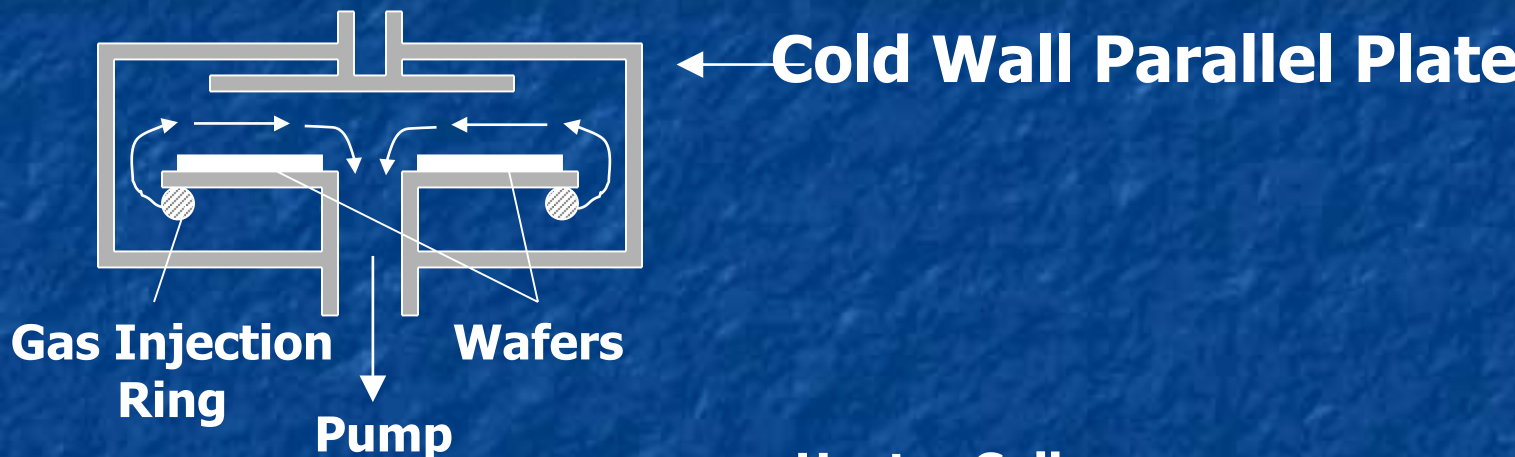
Two types of CVD equipment:

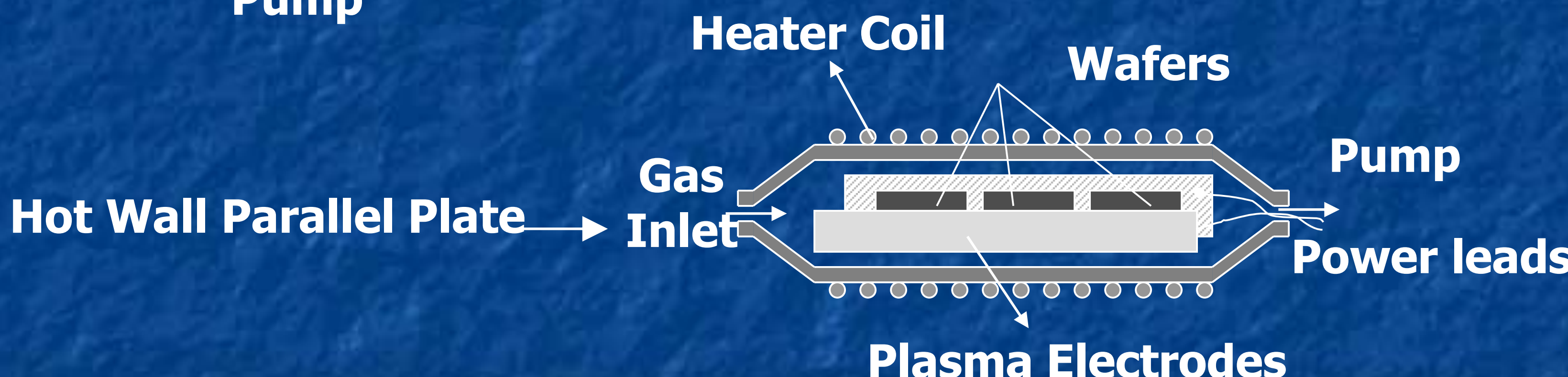
- LPCVD (Low Pressure CVD) : Good uniformity. Used for poly-Si, oxide, nitride.
- PECVD (Plasma Enhanced CVD) : Low temperature process and high deposition rate. Used for oxide, nitride, etc.

Chemical Vapor Deposition (CVD)

LPCVD Systems

Chemical Vapor Deposition (CVD)

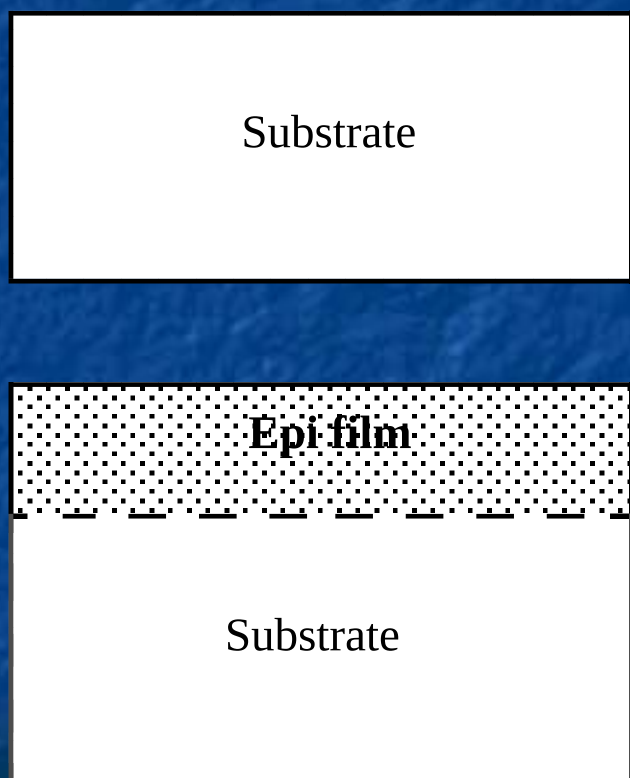




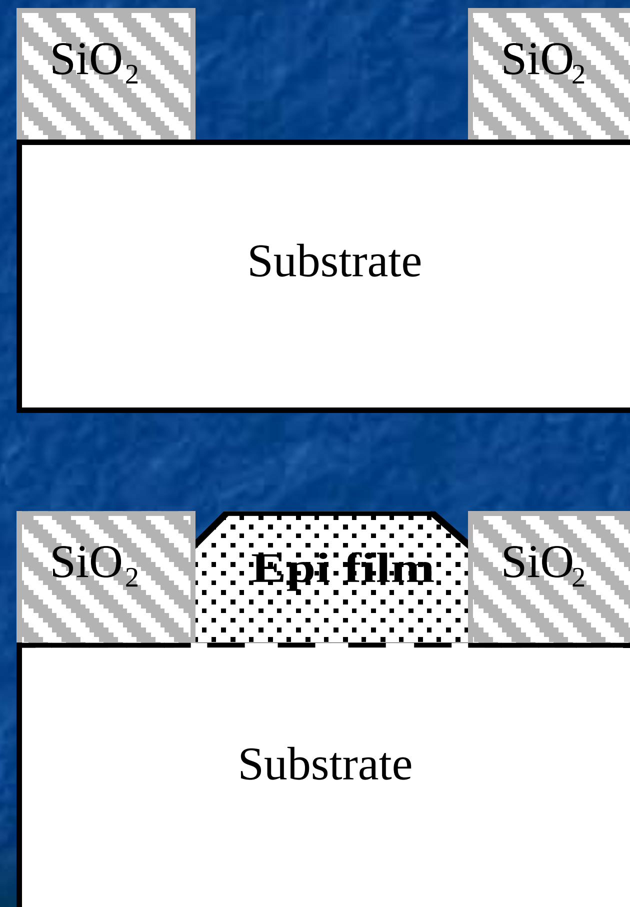
PECVD Systems

Epitaxy *(Deposition of Single-Crystalline Film)*

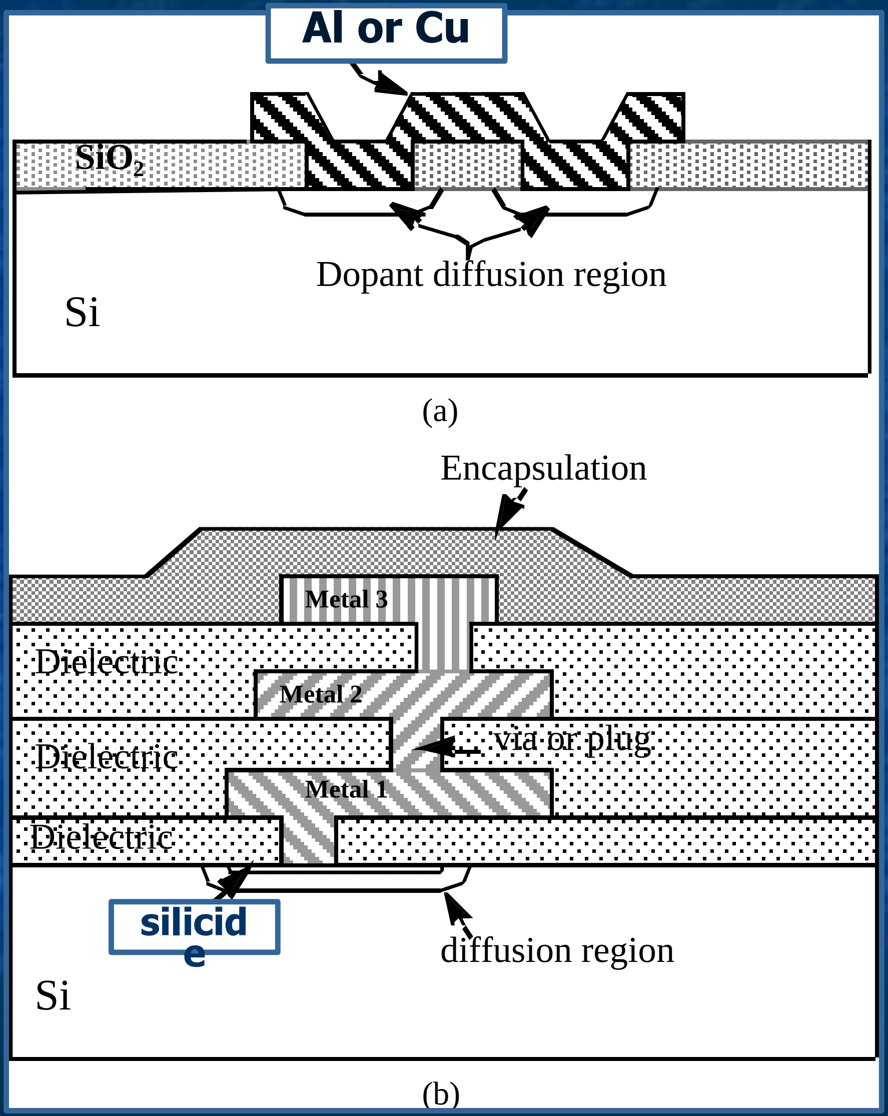
Epitaxy



Selective Epitaxy

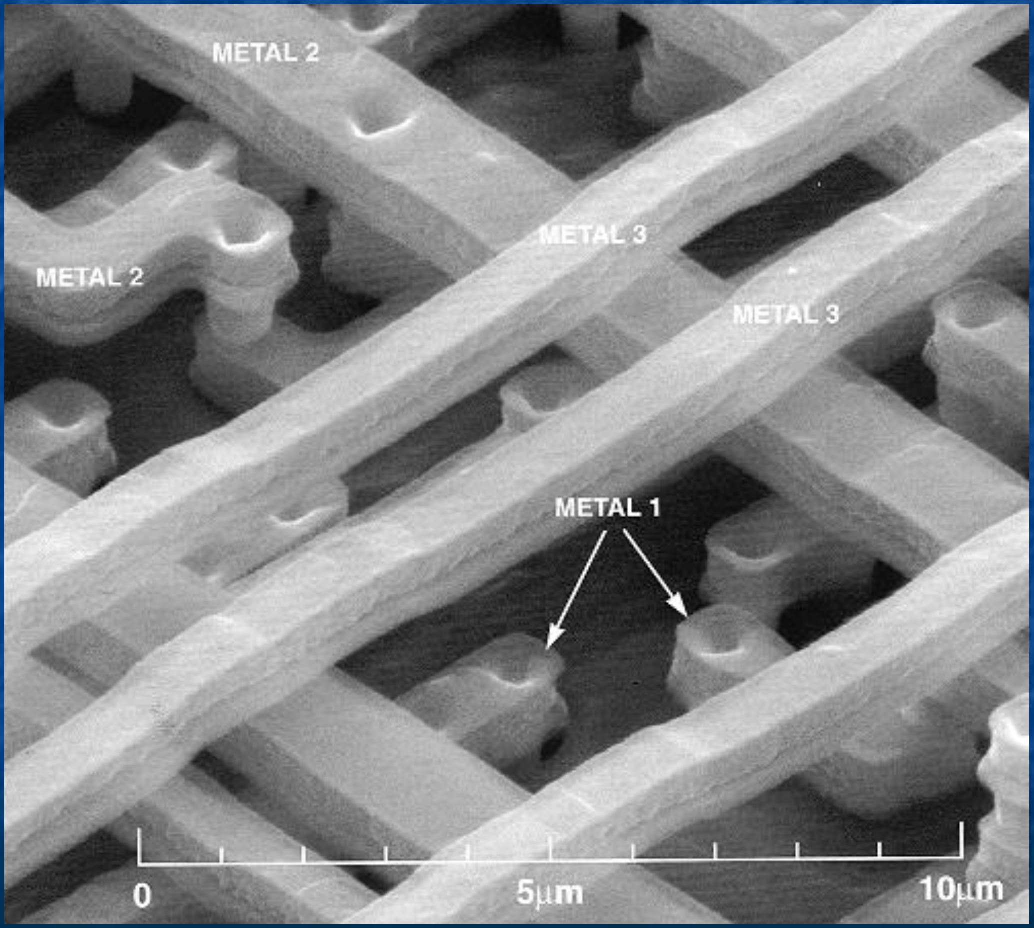


Interconnect – The Back-end Process



Interconnect – The Back-end Process

SEM: Multi-Level Interconnect (after removing the dielectric)



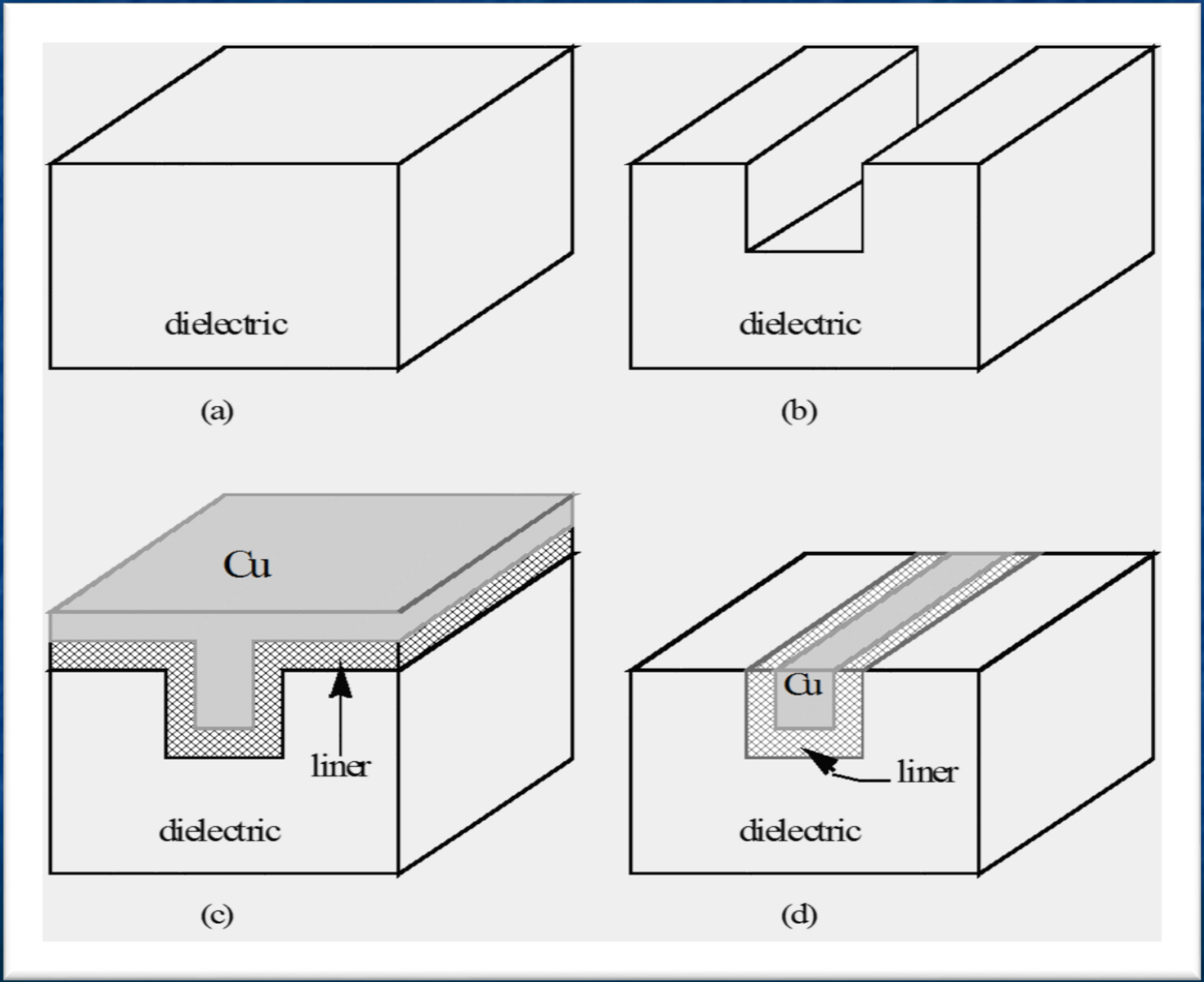
Interconnect – The Back-end Process

Copper Interconnect

- Al interconnect is prone to voids formation by electromigration.
- Cu has excellent electromigration reliability
  and 40% lower resistance than Al.
- Because dry etching of copper is difficult (copper etching products tend to be non-volatile), copper patterns are defined by a *damascene* process.

Interconnect – The Back-end Process

Copper Damascene Process



- **Chemical-Mechanical Polishing (CMP) removes unwanted materials.**
- **Barrier liner prevents Cu diffusion.**

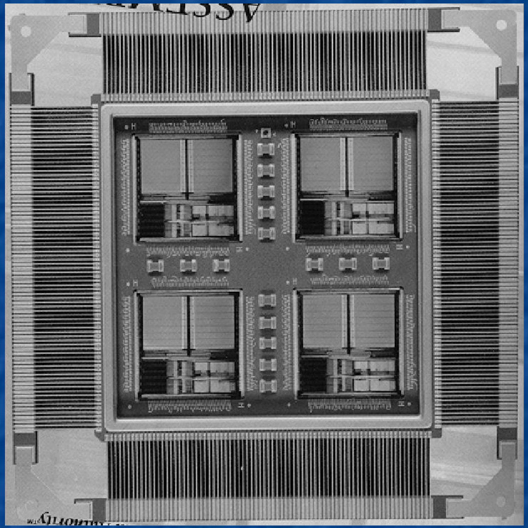
Interconnect – The Back-end Process

Planarization

- A flat surface is highly desirable for subsequent lithography and etching.
- CMP (Chemical-Mechanical Polishing) is used to planarize each layer of dielectric in the interconnect system. Also used in the front-end process.

Testing, Assembly, and Qualification

- Wafer acceptance test
- Die sorting
- Wafer sawing or laser cutting
- Packaging
- Flip-chip solder bump technology
- Multi-chip modules
- Burn-in
- Final test
- Qualification



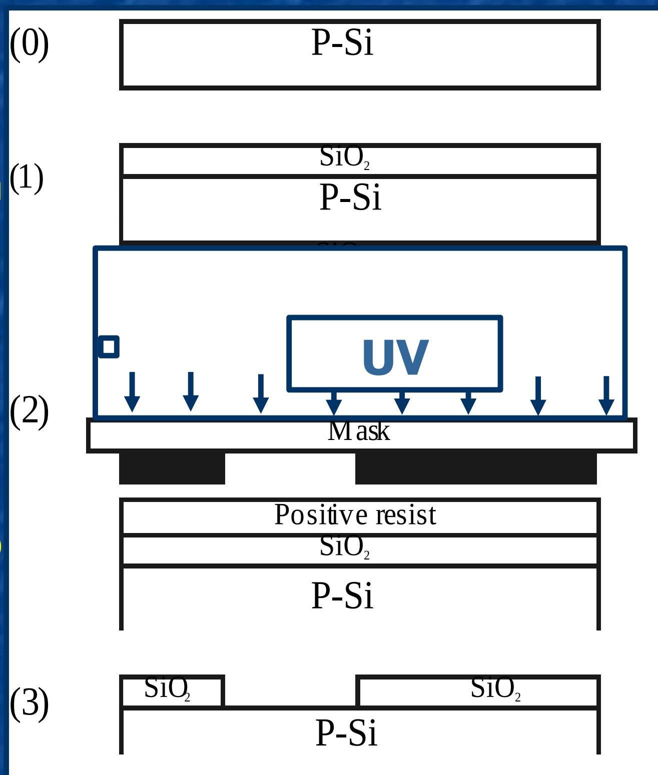
Summary–A Device Fabrication Example

Wafer

Oxidation

Lithograp

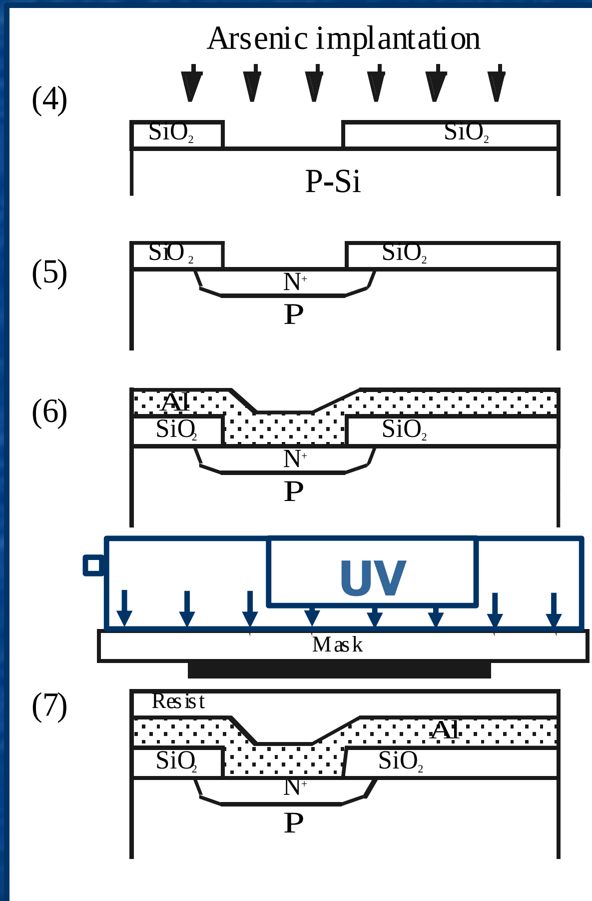
Etching



Ion Implantation

Annealing & Diffusion

Al Sputtering

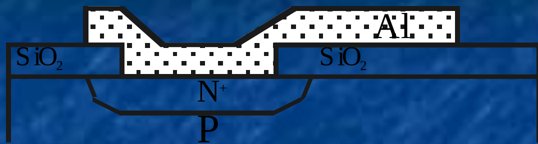


Lithography

Summary–A Device Fabrication Example

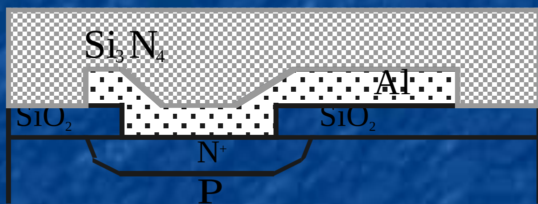
Metal etching

(8)



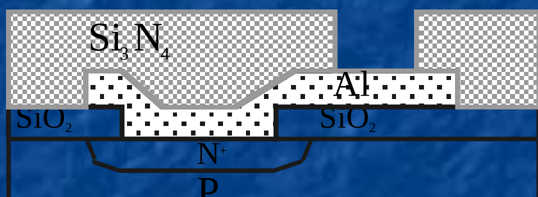
CVD nitride deposition

(9)



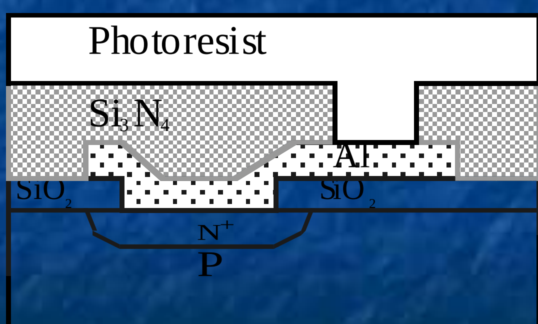
Lithography and etching

(10)



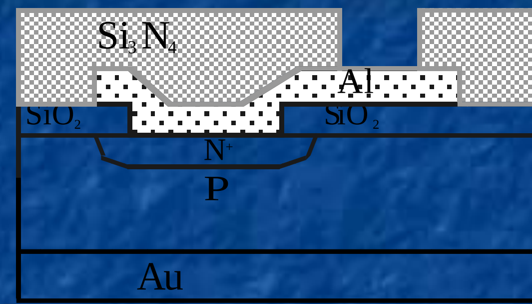
Back Side milling

(11)

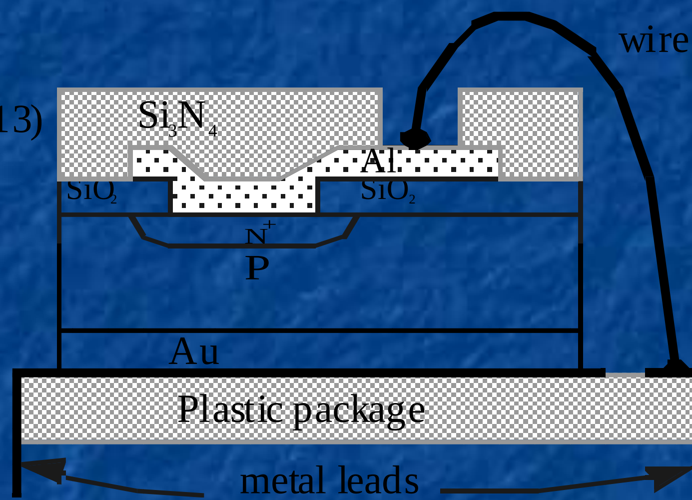


(12)

Back side metallization



(13)



Dicing, wire bonding, and packaging