Introduction to Nanotechnology

- Textbook：
  Nanophysics and Nanotechnology
  by:
  Edward L. Wolf

Instructor: ***H. Hosseinkhani***
E-mail: **hosseinkhani@yahoo.com**

Classroom: A209
Time: Thursday; 13:20-16:10 PM
Office hour: Thur., 10:00-11:30 AM or by appointment

Sep 15	Introduction	Hossein
Sep 22	Systematic of Making Things Smaller	Hossein
Sep 29	What are limits to smallness	Hossein
Oct 6	Quantum Nature of the Nanoworld	CW Chen
Oct 13	Quantum Consequence for the Macroworld	CW Chen
Oct 20		
Oct 27	Self-Assmbled Nano-Straucture in Nature and Industry	Hossein
Nov 3		
Nov 10	**Midterm**	
Nov 17	Physics-based Experimental Approaches to Nanofabrication and Nanotechnology	Hossein
Nov 24		
Dec 1	Quantum Technologies based on Magnetism, Electron and Nuclear Spin, and Superconductivity	KH Chen
Dec 8		
Dec 15	Silicon Nanoeletronic and Beyond	Hossein
Dec 22		
Dec 29	Looking into the Future	LC Chen
Jan 5		
Jan 12	**Final Exam**	

Objective of the course

The course, Introduction to Nanotechnology (IN), will focus on understanding of the basic molecular structure principals of Nano-materials. It will address the molecular structures of various materials. The long term goal of this course is to teach molecular design of materials for a broad range of applications. A brief history of biological materials and its future perspective as well as its impact to the society will be also discussed.

Evaluation; Score: 100%:

Mid-term Exam: 30%
Final Exam: 30%
Scientific Activity: 40 % (Home work, Innovation Design)

Contents

- Introduction (*Prof. Hossein*)
- Systematic of Making Things Smaller (*Prof. Hossein*)
- What are limits to smallness (*Prof. Hossein*)
- Quantum Nature of the Nano-world (*Prof. CW Chen*)
- Quantum Consequence for the Macro-world (*Prof. CW Chen*)
- Self-Assembled Nano-Structure in Nature and Industry (*Prof. Hossein*)
- Physical-based Experimental Approaches to Nanofabrication and Nanotechnology (*Prof. Hossein*)

- Mid-term Exam

Contents

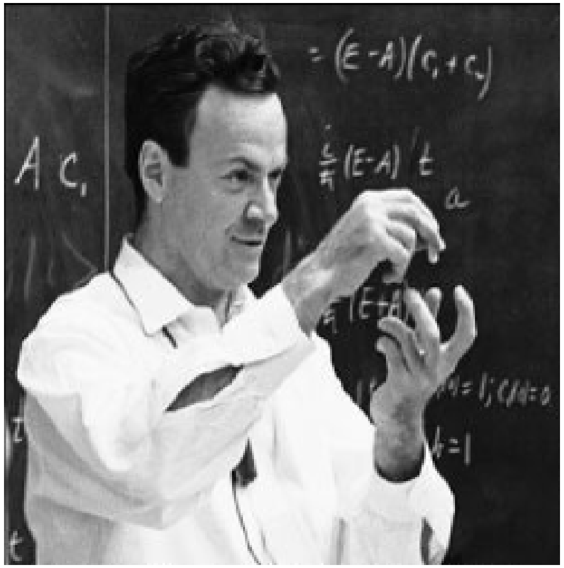
- Quantum Technologies based on Magnetism, Electron and Nuclear Spin, and Superconductivity (*Prof. KH Chen*)
- Silicon Nanoeletronic and Beyond (*Prof. Hossein*)
- Looking into the Future (*Prof. LC Chen*)

- Final Exam

Silicon Nanoeletronic and Beyond

Subjects: Today class

1. **Silicon Nano-CMOS**
2. **Oxide Nano-Electronic**
3. **Transistors**



The year was 1959….

At a meeting of the American Physical Society , the famous scientist, Richard Feynman asked a question:

Why cannot we write the entire 24 volumes of the Encyclopedia Britannica on the head of a pin?”

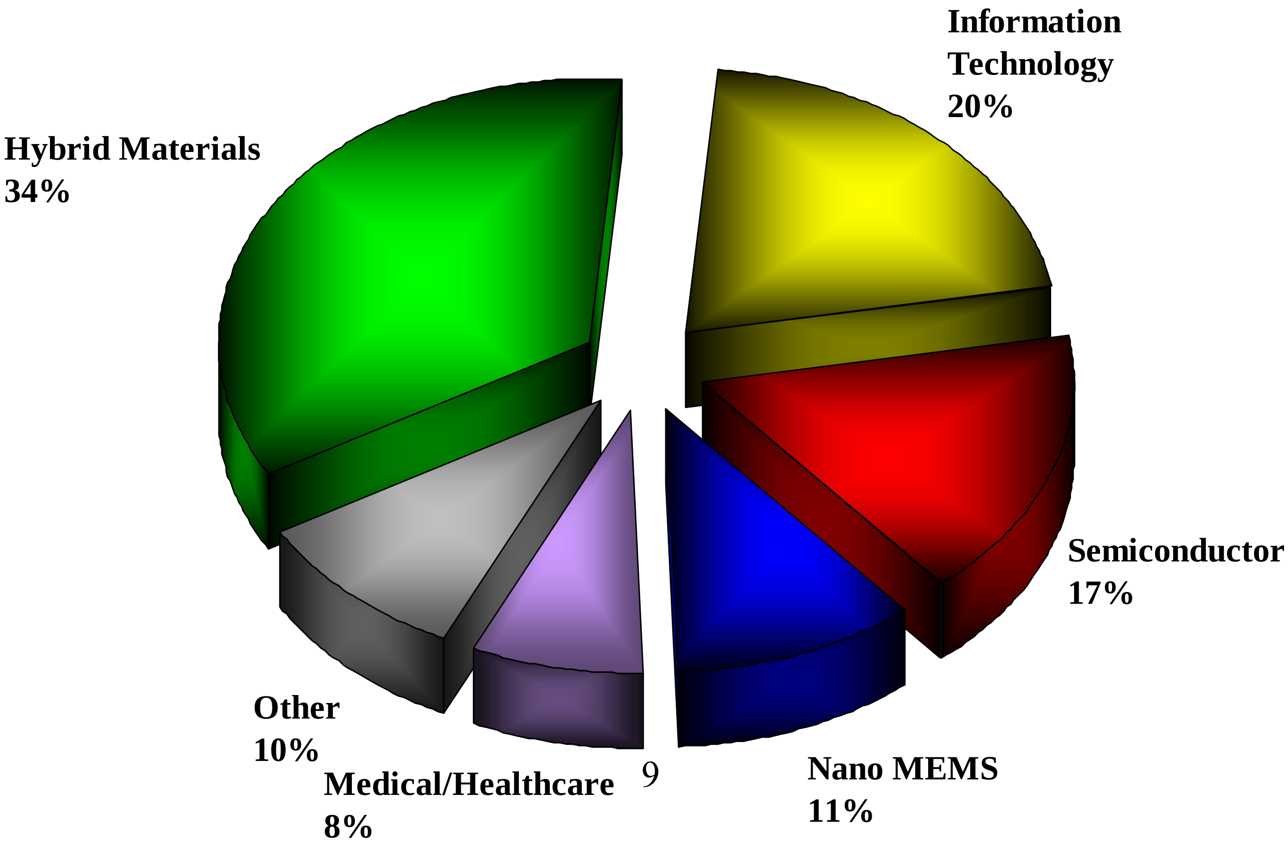
That speech, with its famous sentence “*there is plenty of room at the bottom” is generally recognized as the manifesto of* Nanotechnology.

Today, a NAND Flash of 4GB can hold approximately 100-200 thousand pages of text and illustrations, that is roughly 1000 pages/mm^2

I. Nanoelectronics Era

Nanotechnology:

- Nanotechnology scale: 1nm (0.1nm) ~ 100nm
- Nanotechnology Industry Focus:
  Nanoelectronics (IT+Semicon.+NEMS)=48%



I. Nanoelectronics Era

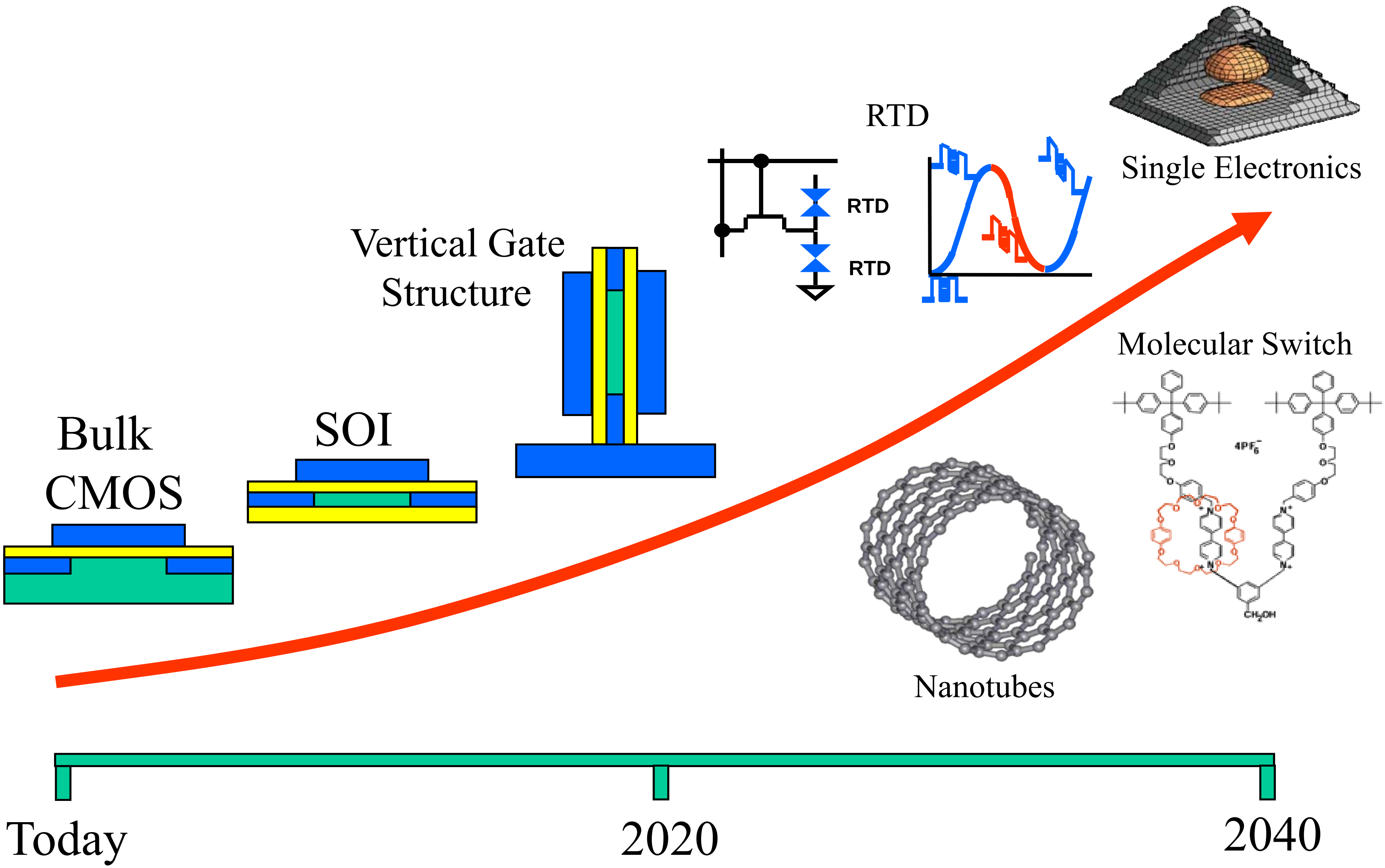
Great Nanoelectronics Area

1. **Silicon Nano-CMOS**

2. **Non-Silicon Nano-electronics**

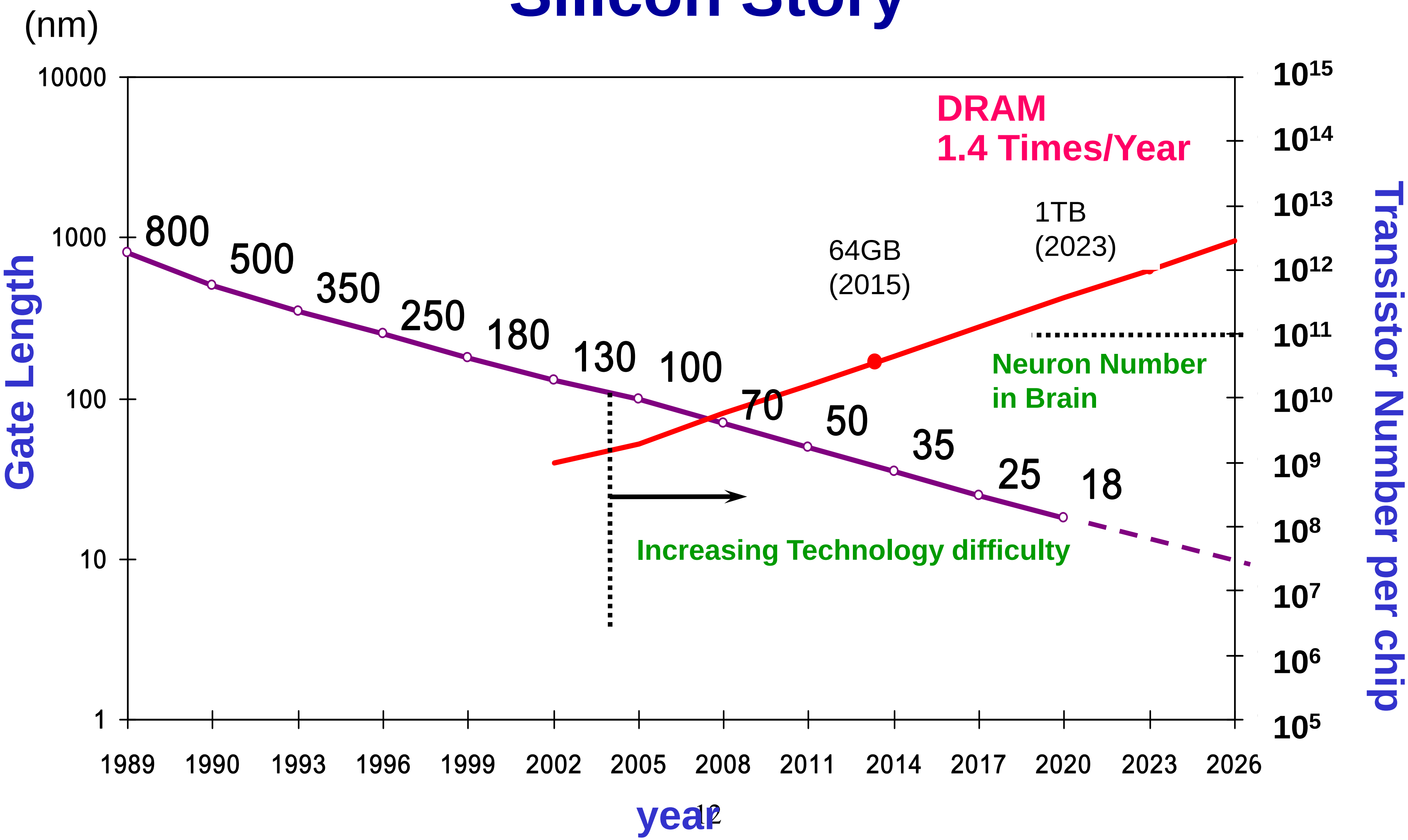
CMOS is referred to as:
complementary-symmetry
metal–oxide– semiconductor

I. Nanoelectronics Era



II. Challenges of Silicon Nanoelectronics — Nano-CMOS

Silicon Story



II. Challenges of Silicon Nanoelectronics — Nano-CMOS

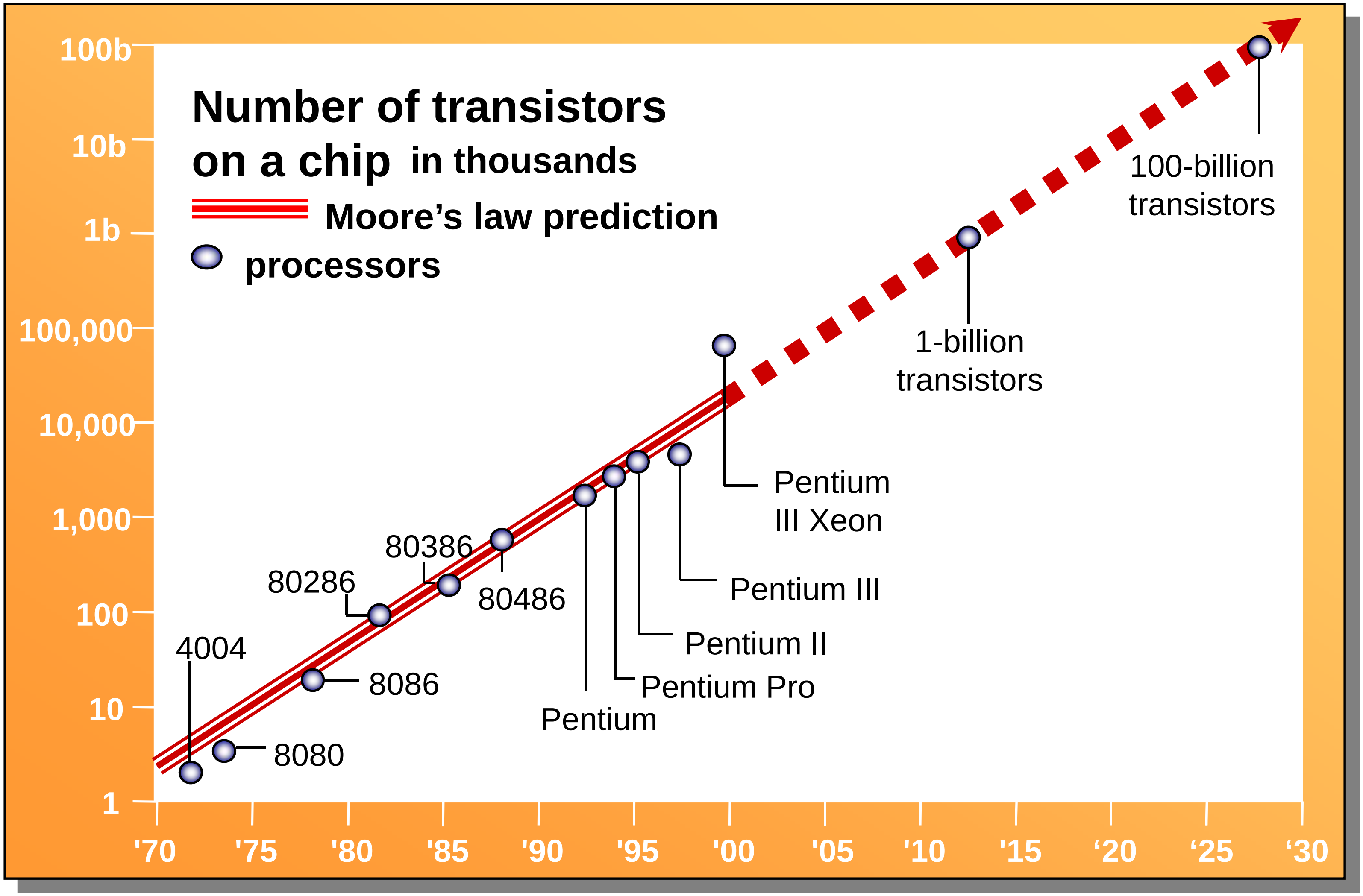
CMOS Scaling Challenges

High Performance Logic Technology Requirements—2001 ITRS

CALENDAR YEAR	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
TECHNOLOGY NODE (NM0	130			90			65	45	32	22
MPU GATE LENGTH	65	53	45	37	32	30	25	18	13	9
Gate Dielectric Equivalent Oxide Thickness (EOT) (nm) [1]	1.45	1.35	1.35	1.15	1.05	0.95	0.85	0.65	0.50	0.45
Electrical Thickness Adjustment Factor (Gate Depletion and Quantum Effects) (nm) [2]	0.8	0.8	0.8	0.8	0.8	0.8	0.5	0.5	0.5	0.5
Tox Electrical Equivalent (nm) [3]	2.25	2.15	2.15	1.95	1.85	1.75	1.35	1.15	1.00	0.95
Vdd (V) [4]	1.2	1.2	1.1	1.0	0.9	0.9	0.8	0.6	0.5	0.4

II. Challenges of Silicon Nanoelectronics — Nano-CMOS

CPU with Multimedia Capability



II. Challenges of Silicon Nanoelectronics — Nano-CMOS

Integration Revolution — A Monster

2020 0.018μm Ultimate Generation?

2020 – 2040 or 2050 Integration Continues.

2015 64GB DRAM

1-Billion-Tx CPU (SOC)

2025 1TB DRAM VDD=0.6V, V_T=0.1V

100-Billion-Tx CPU (SOC) $I_G \sim \mu A$

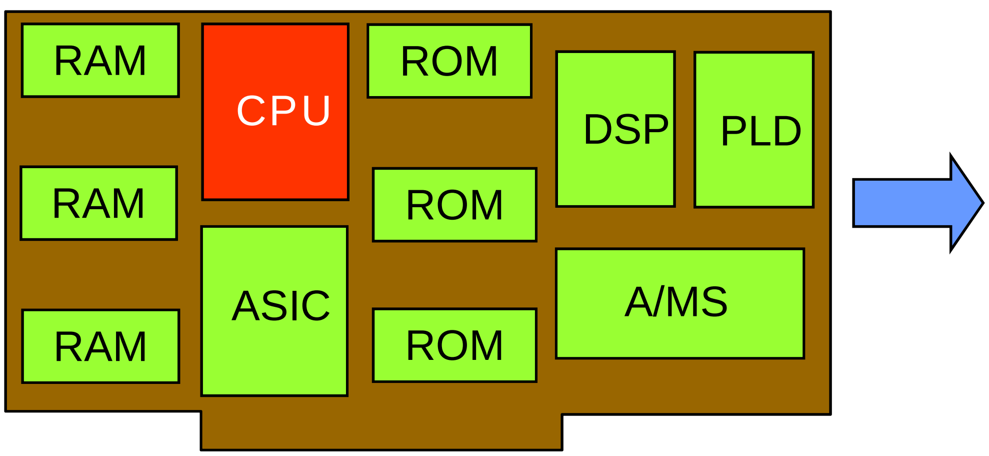
2050 32TB DRAM VDD<0.6V, V_T=0.1V

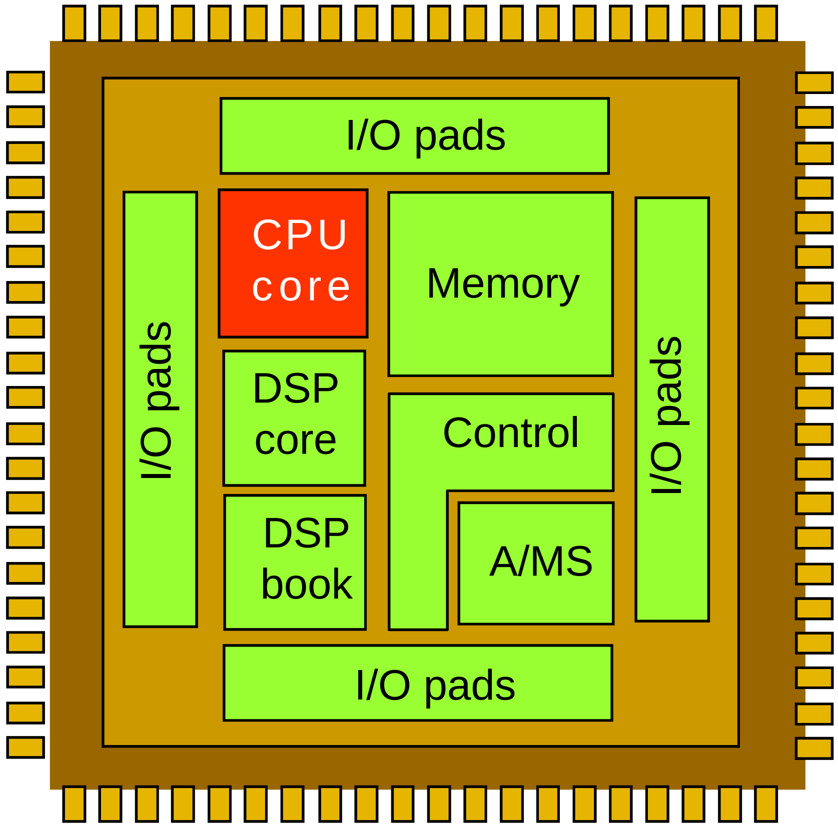
4-Trillion-Tx CPU (SOC) $I_G \sim \mu A$

II. Challenges of Silicon Nanoelectronics — Nano-CMOS

Is it possible to design a 100-Billion-Transistor SOC in 100 Days?

A/MS=analog/mixed signal
ASIC = application-specific IC
CPU = central processing unit
PLD = programmable logic device





Board components

Virtual components

II. Challenges of Silicon Nanoelectronics — Nano-CMOS

Silicon Nano-CMOS

- Process Technologies and Devices

  100 nm : Brick Wall.

  50 nm : Iron Wall ?

  10 nm : Steel Wall ?

  6 nm : Galaxy Wall ?

- Architectures, Integration, and Applications

  Multimedia CPU with 100 billion transistors

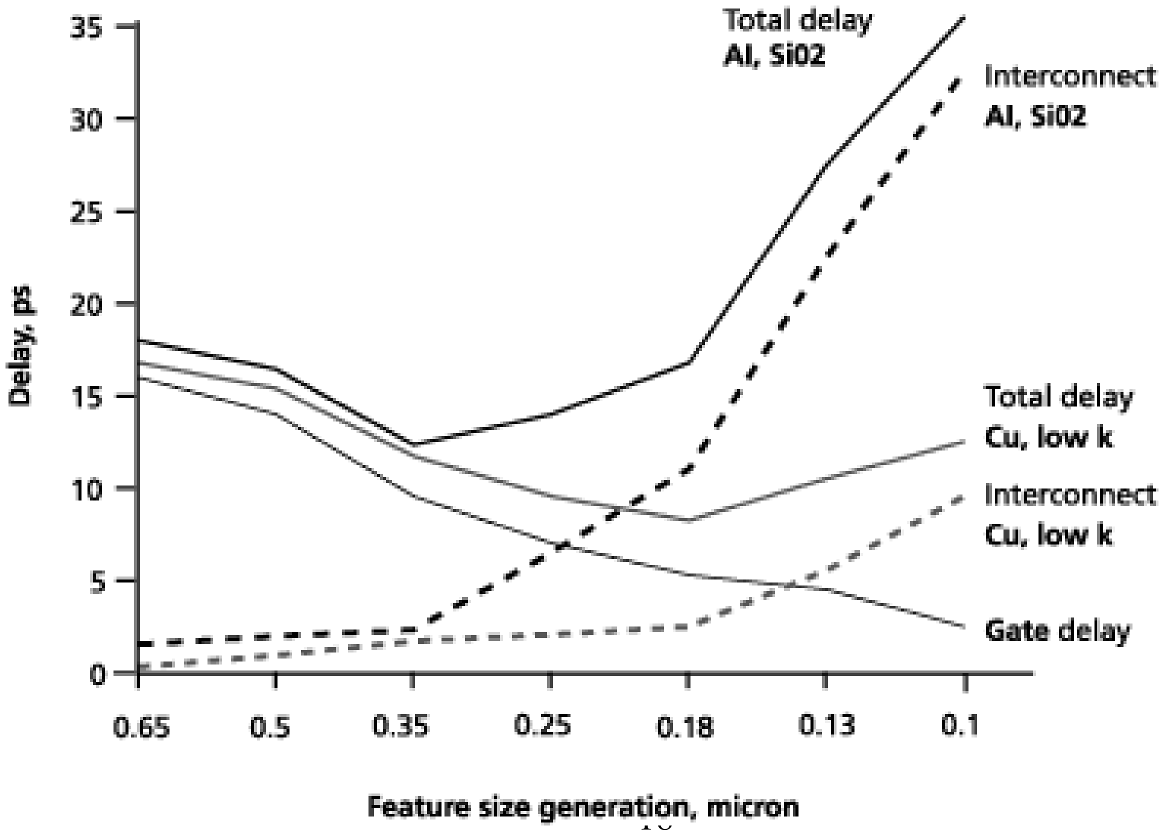
  Tera-Bit DRAM

  Nano-SOC

II. Challenges of Silicon Nanoelectronics — Nano-CMOS

Research Challenges:

1. Interconnect Modeling and designing



II. Challenges of Silicon Nanoelectronics — Nano-CMOS

Research Challenges (cont'd):

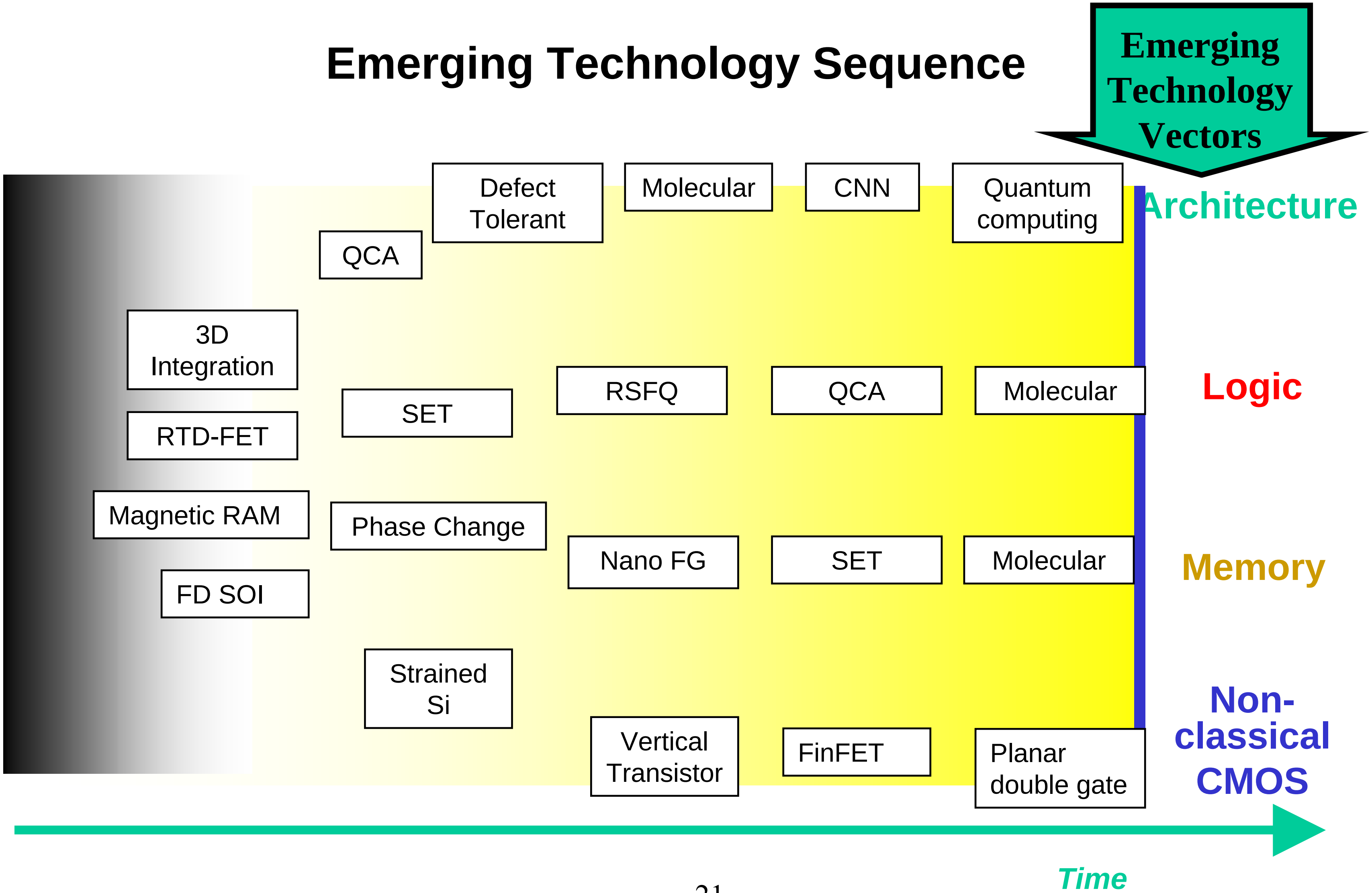
2. Ultra-low-power (ULP) low-voltage (LV) but high-speed high-frequency analog/digital IPs
3. Programmability in IP/whole-chip design and verification

II. Challenges of Silicon Nanoelectronics — Nano-CMOS

Research Challenges (cont'd):

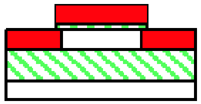
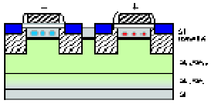
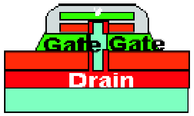
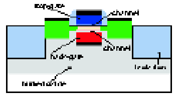
4. Embedded software to make SOCs fit future needs in many major intelligent applications
5. Fast design cycle

III. Grand Challenges of Non-Silicon Nanoelectronics



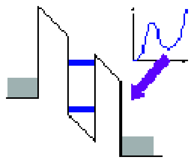
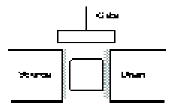
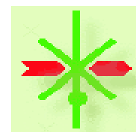
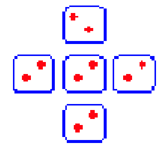
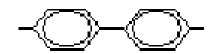
III. Grand Challenges of Non-Silicon Nanoelectronics

Table 2. Nonclassical CMOS

					
DEVICE	ULTRA-THIN BODY SOI	BAND-ENGINEERED TRANSISTOR	VERTICAL TRANSISTOR	FINFET	DOUBLE-GATE TRANSISTOR
CONCEPT	Fully depleted SOI	SiGe or Strained Si channel; bulk Si or SOI	Double-gate or surround-gate structure (No specific temporal sequence for these three structures is intended)		
APPLICATION/DRIVER	Higher performance, Higher transistor density, Lower power dissipation				
ADVANTAGES	-Improved subthreshold slope -V_t controllability	-Higher drive current -Compatible with bulk and SOI CMOS	-Higher drive current -Lithography independent L_g	-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND	-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND
SCALING ISSUES	-Si film thickness -Gate stack -Worse short channel effect than bulk CMOS	-High mobility film thickness, in case of SOI -Gate stack -Integration	-Si film thickness -Gate stack -Integrability -Process complexity -Accurate TCAD including QM effect	-Si film thickness -Gate stack -Process complexity -Accurate TCAD including QM effect	-Gate alignment -Si film thickness -Gate stack -Integrability -Process complexity -Accurate TCAD including QM effect
DESIGN CHALLENGES	-Device characterization -Compact model and parameter extraction	-Device characterization	-Device characterization -PD versus FD -Compact model and parameter extraction -Applicability to mixed signal applications		
MATURITY	Development				
TIMING	Near Future →				

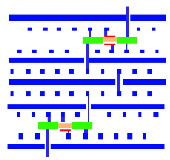
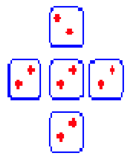
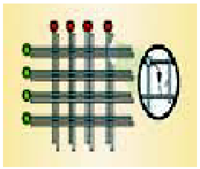
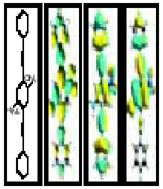
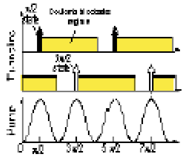
III. Grand Challenges of Non-Silicon Nanoelectronics

Table 4. Emerging Logic Devices

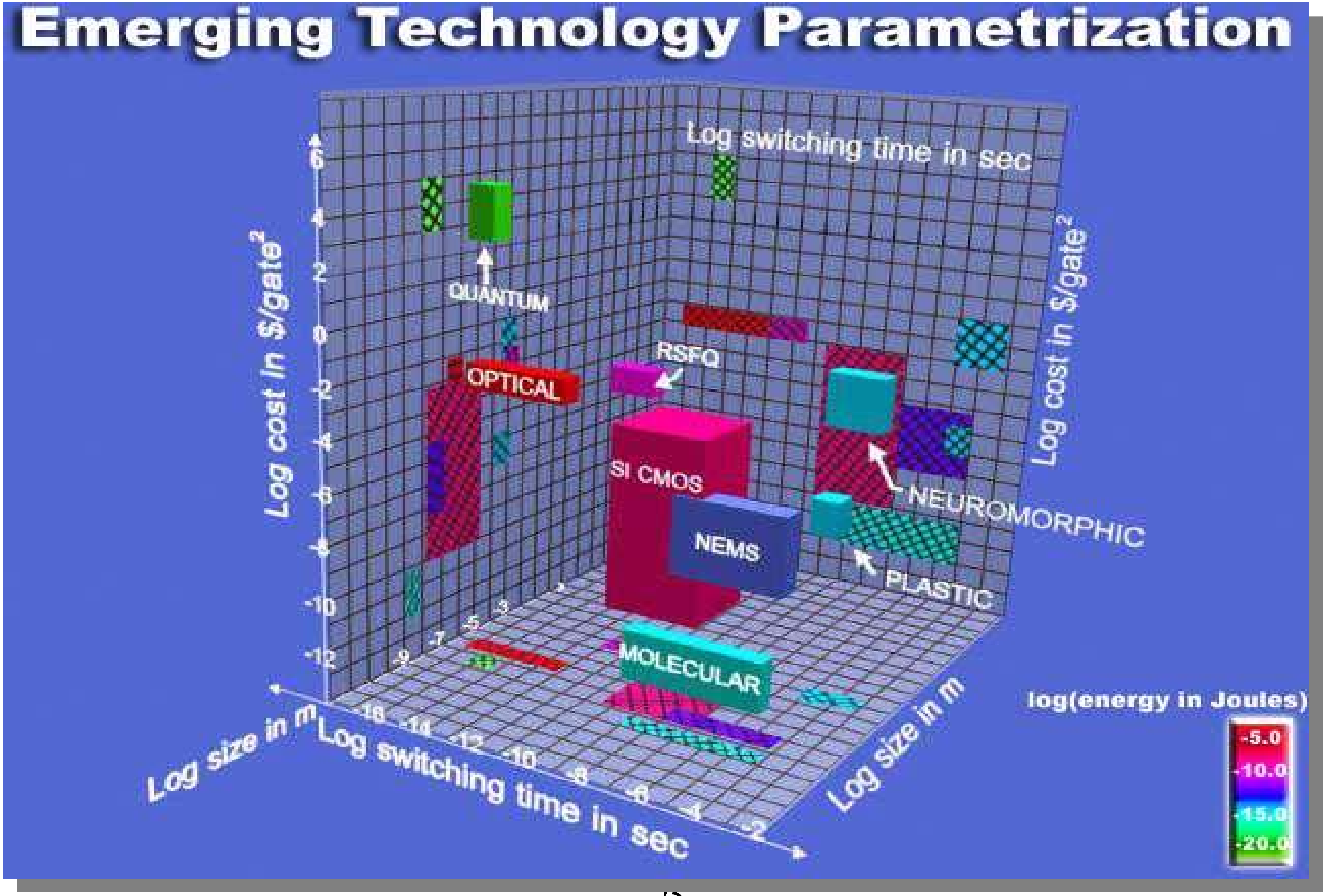
						
DEVICE	RESONANT TUNNELING DIODE - FET	SINGLE ELECTRON TRANSISTOR	RAPID SINGLE QUANTUM FLUX LOGIC	QUANTUM CELLULAR AUTOMATA	NANOTUBE DEVICES	MOLECULAR DEVICES
TYPES	3-Terminal	3-Terminal	Josephson Junction +Inductance Loop	-Electronic QCA -Magnetic QCA	FET	2-Terminal and 3-Terminal
ADVANTAGES	Density, Performance, RF	Density, Power, Function	High Speed, Potentially Robust, (Insenstive to Timing Error)	High Functional Density, No Interconnect in Signal Path, Fast and Low Power	Density, Power	Identity of Individual Switches (e.g., Size, Properties on Sub-nm Level. Potential Solution to Interconnect Problem
CHALLENGES	Matching of Device Properties Across Wafer	New Device and System, Dimensional Control (e.g., Room Temp Operation), Noise (Offset Charge), Lack of Drive Current	Low Temperatures, Fabrication of Complex, Dense Circuitry	Limited Fan Out, Dimensional Control (Room Temperature Operation), Architecture, Feedback from Devices, Background Charge	New Device and System, Difficult Route for Fabricating Complex Circuitry	Thermal and Environmental Stability, Two Terminal Devices, Need for New Architectures
MATURITY	Demonstrated	Demonstrated	Demonstrated	Demonstrated	Demonstrated	Demonstrated

III. Grand Challenges of Non-Silicon Nanoelectronics

Table 6. Emerging Research Architectures

						
ARCHITECTURES	3-D INTEGRATION	QUANTUM CELLULAR AUTOMATA	DEFECT TOLERANT ARCHITECTURE	MOLECULAR ARCHITECTURE	CELLULAR NONLINEAR NETWORKS	QUANTUM COMPUTING
DEVICE IMPLEMENTATION	CMOS with Dissimilar Material Systems	Arrays of Quantum Dots	Intelligently Assembles Nanodevices	Molecular Switches and Memories	Single Electron Array Architectures	Spin Resonance Transistors, NMR Devices, Single Flux Quantum Devices
ADVANTAGES	Less Interconnect Delay, Enables Mixed Technology Solutions	High Functional Density. No Interconnects in Signal Path	Supports Hardware with Defect Densities >50%	Supports Memory Based Computing	Enables Utilization of Single Electron Devices at Room Temperature	Exponential Performance Scaling, Enables Unbreakable Cryptography
CHALLENGES	Heat Removal, No Design Tools, Difficult Test and Measurement	Limited Fan out, Dimensional Control (Low Temperature Operation), Sensitive to Background Charge	Requires Pre-Computing Test	Limited Functionality	Subject to Background Noise, Tight Tolerances	Extreme Application Limitation, Extreme Technology
MATURITY	Demonstration	Demonstration	Demonstration	Concept	Demonstration	Concept

III. Grand Challenges of Non-Silicon Nanoelectronics



III. Grand Challenges of Non-Silicon Nanoelectronics

Grand Challenges :

1. **Reliable signal input/output and interconnection for nanodevices/nanostructures**

2. **Stable, reproducible, and low-cost nanofabrication process for mass production with reasonable yield**

III. Grand Challenges of Non-Silicon Nanoelectronics

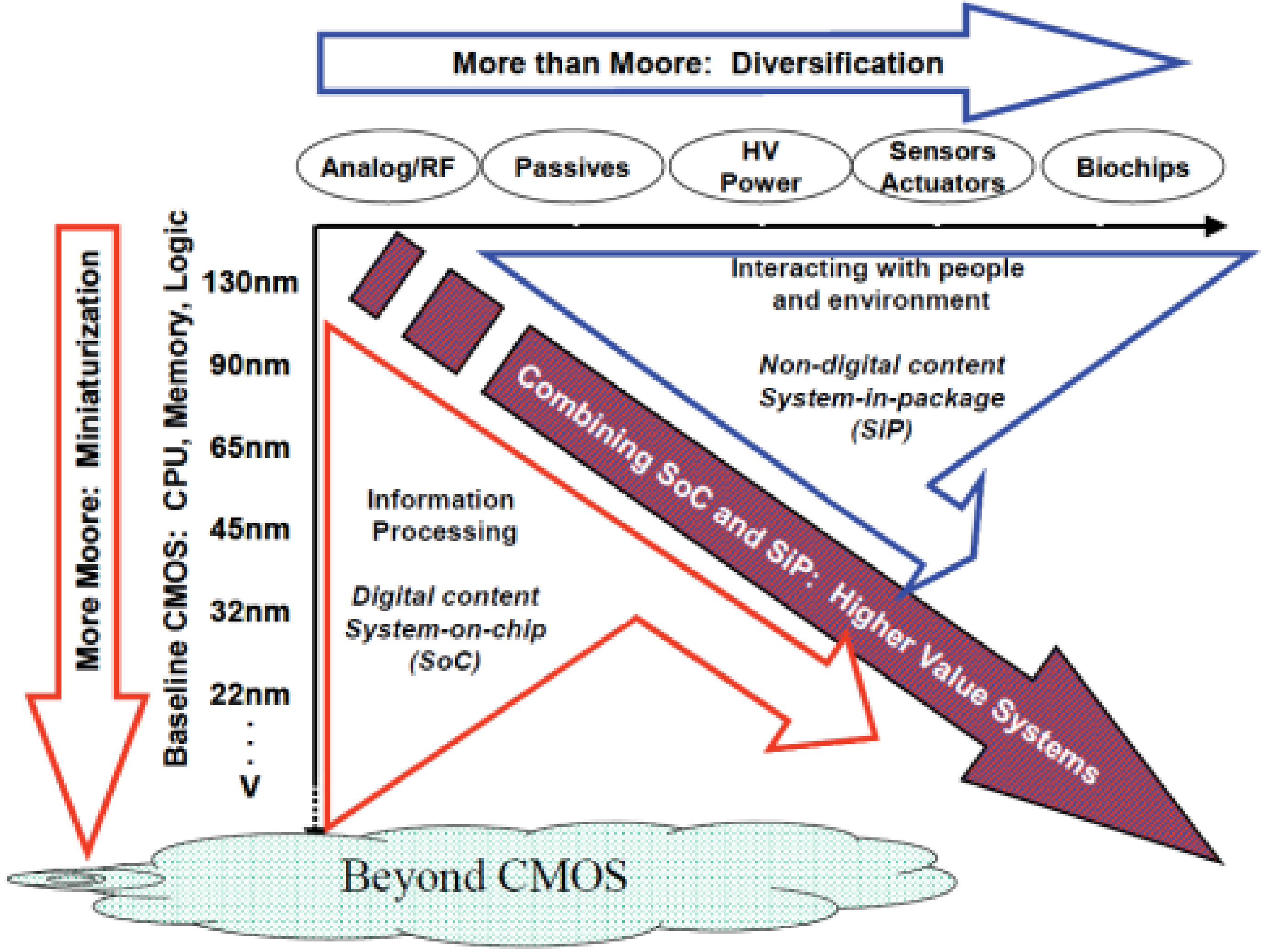
Grand Challenges (cont'd):

3. **New nanoelectronic circuits, systems, architectures, and design methodologies for nano-integration**

4. **Verification, testing, and packaging methods for nano-system chips**

5. **Fundamental quantum physics in the atomic or molecule level**

Semiconductor Roadmap



From International Technology Roadmap for Semiconductors (2007): http://www.itrs.net

Oxides and Semiconductors

- Three main properties of semiconductors (Si) essential for technological applications
  1. Conductivity can be tuned over a wide range by either doping or field effect
     - Semiconductors √
     - Oxides √
  2. Insulating layers (SiO_2) can be formed readily, enabling field-effect devices to be created
     - Semiconductors √
     - Oxides √
  3. Devices can be reduced in size to nanoscale dimensions
     - Semiconductors √
     - Oxides √

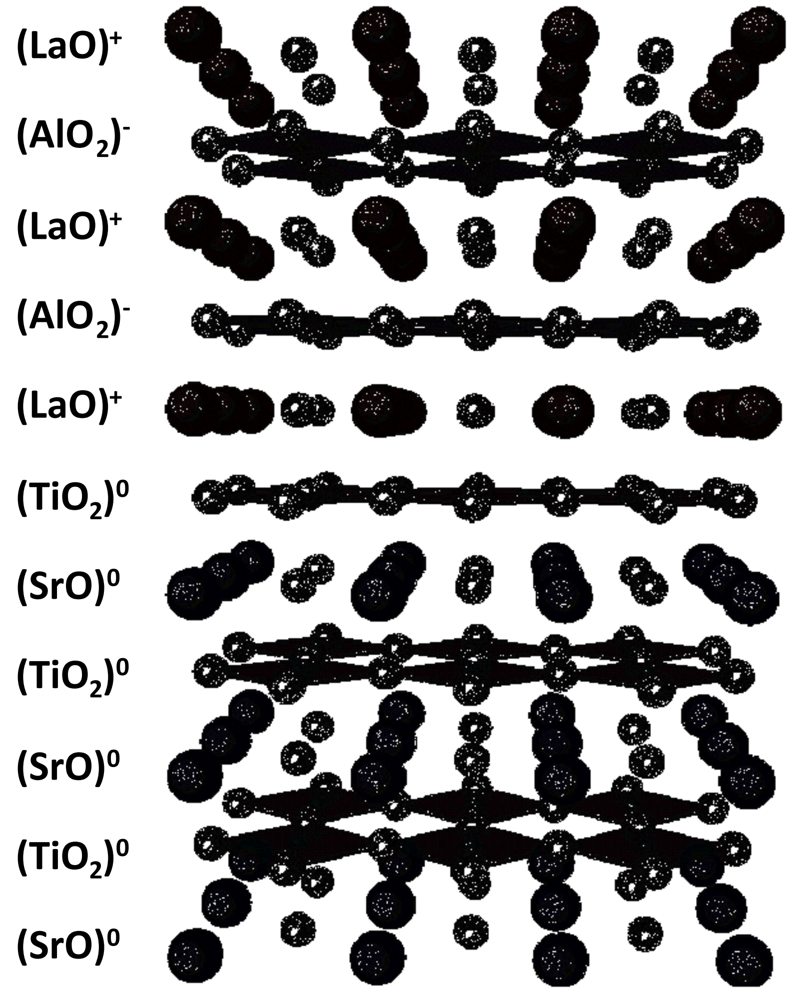
Complex Oxides

- Ferroelectricity / Piezoelectricity
  - $BaTiO_3$, Strained $SrTiO_3$, $(Pb,Zr)TiO_3$
- Ferromagnetism
  - $SrRuO_3$, LSMO

- Colossal Magnetoresistance
  - $(La,Sr)MnO_3$
- Superconductivity
  - $YBa_2Cu_3O_7$
  - $SrTiO_3$

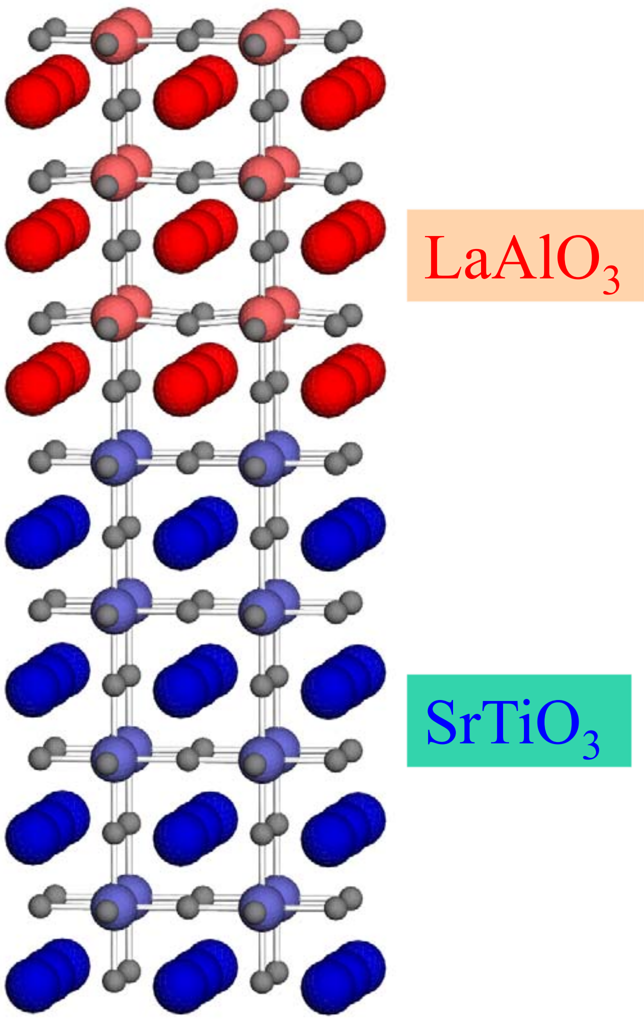
Emergent Phenomena at Oxide Interfaces

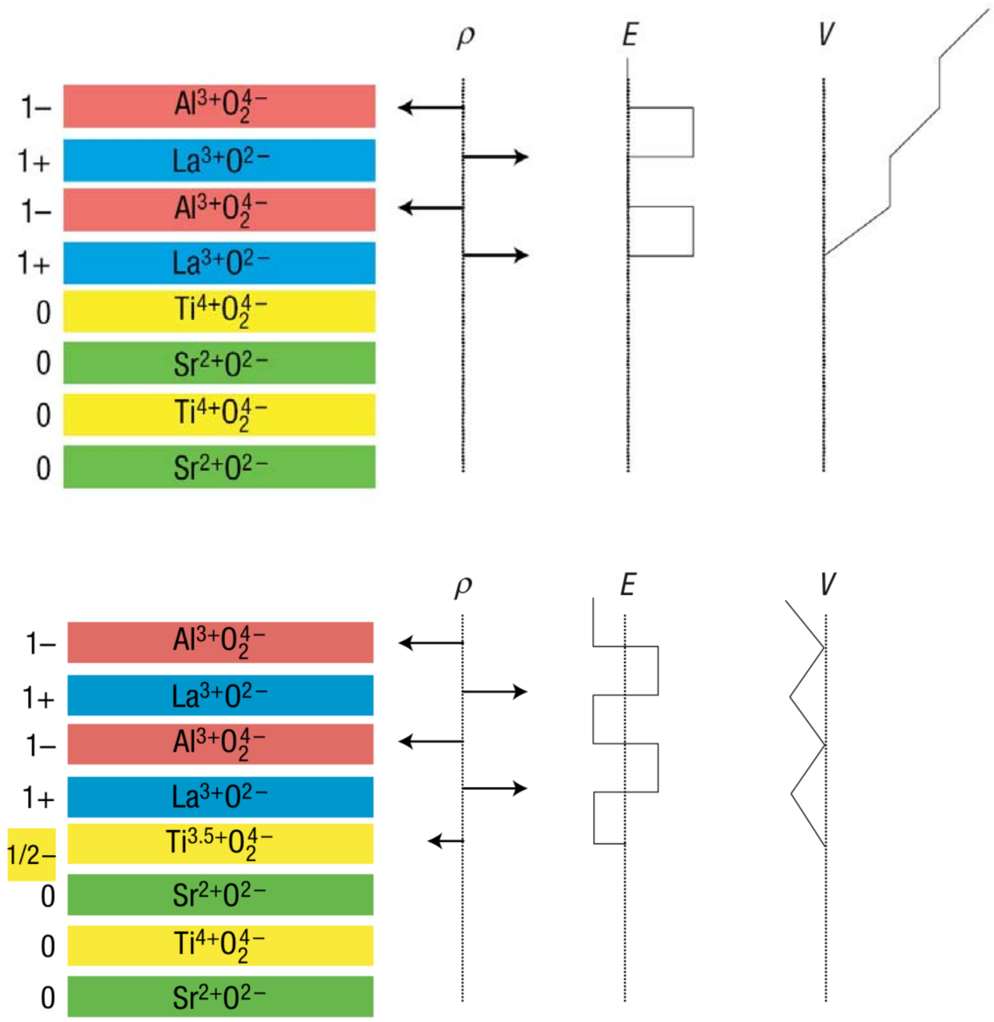
- High-mobility 2DEG
  - Ohtomo and Hwang, Nature (2004)
- Metal-insulator transition
  - Thiel et al, *Science* (2006)
- Superconductivity
  - Reyren et al, *Science* (2007); Caviglia, *Nature* (2008)
- Magnetism
  - Brinkman et al, *Nature Materials* (2007)



$LaAlO_3/SrTiO_3$

Polar Discontinuity: $LaAlO_3$ / $SrTiO_3$





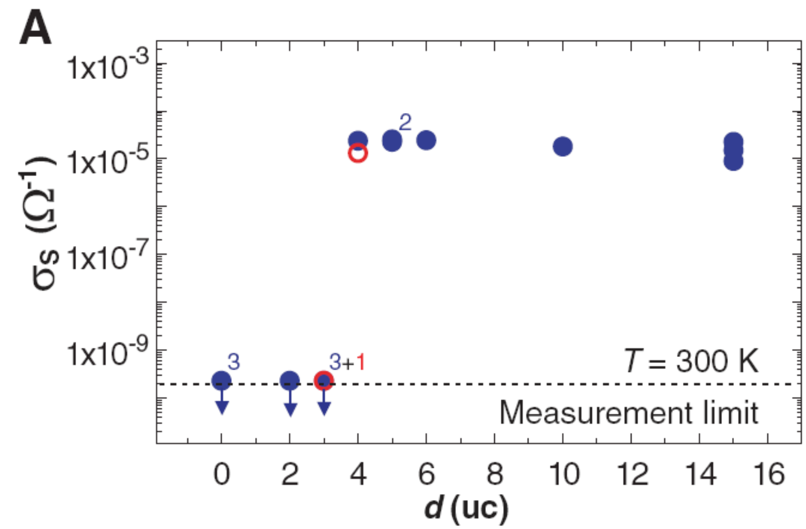
Nakagawa, Hwang, and Muller, *Nature Materials* **5**, 204 (2006)

Metal-Insulator Transition

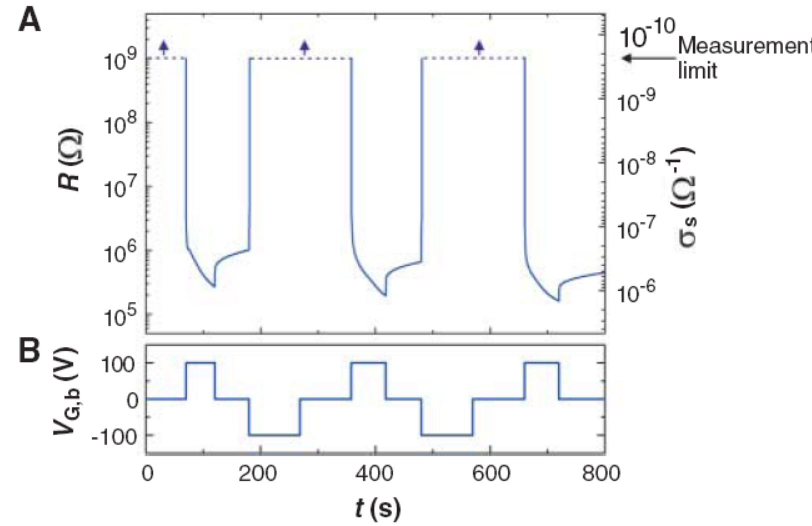
Tunable Quasi–Two-Dimensional Electron Gases in Oxide Heterostructures

S. Thiel,[1] G. Hammerl,[1] A. Schmehl,[2] C. W. Schneider,[1] J. Mannhart[1]*

29 SEPTEMBER 2006 VOL 313 SCIENCE www.sciencemag.org



- Electric-field driven phase transition
- Voltage applied across $SrTiO_3$ substrate
- Critical thickness
  - ~ 3 unit cells $LaAlO_3$

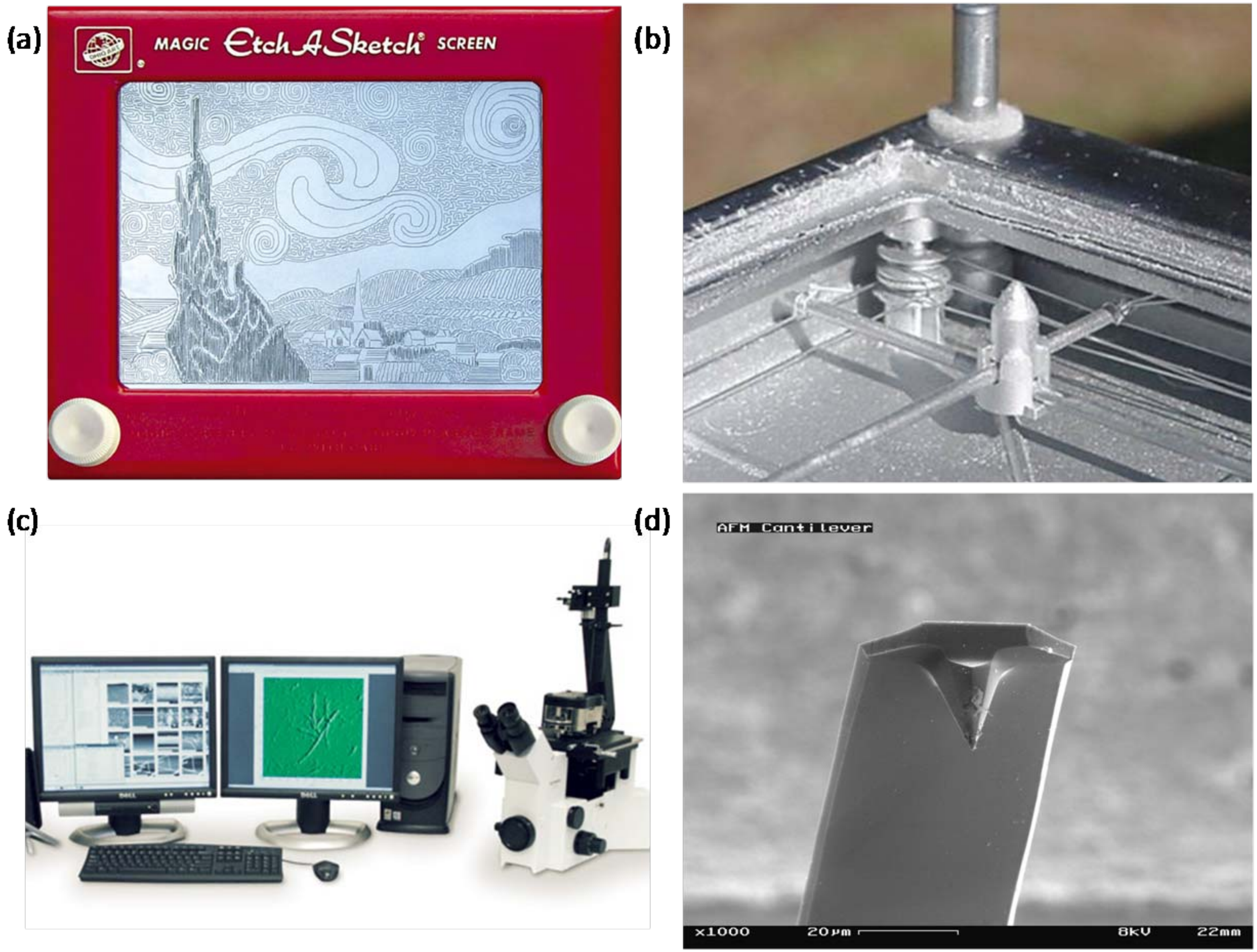


$LaAlO_3/SrTiO_3$

Etch-a-Sketch Nanoelectronics

Toy

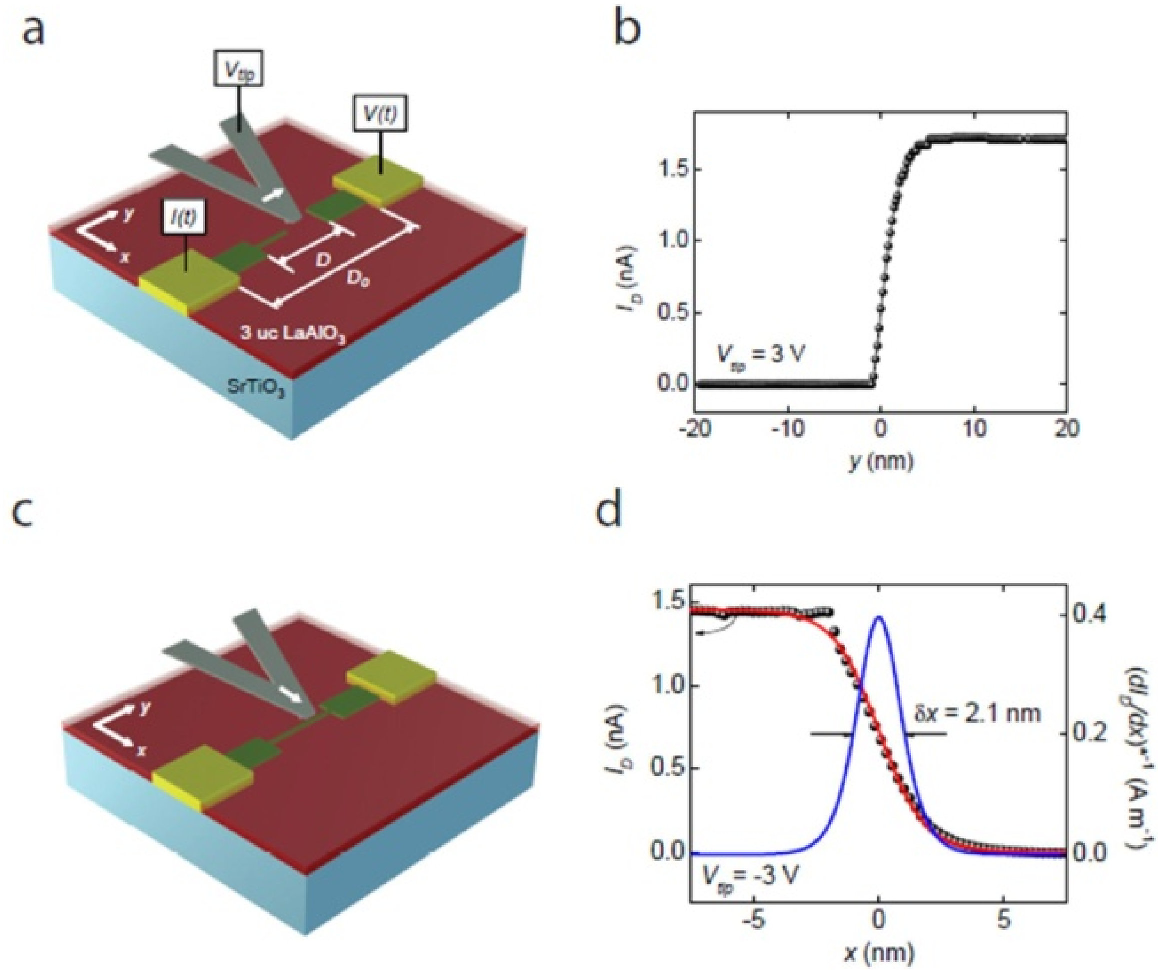
Tool



Conducting AFM Lithography of $LaAlO_3/SrTiO_3$

Writing

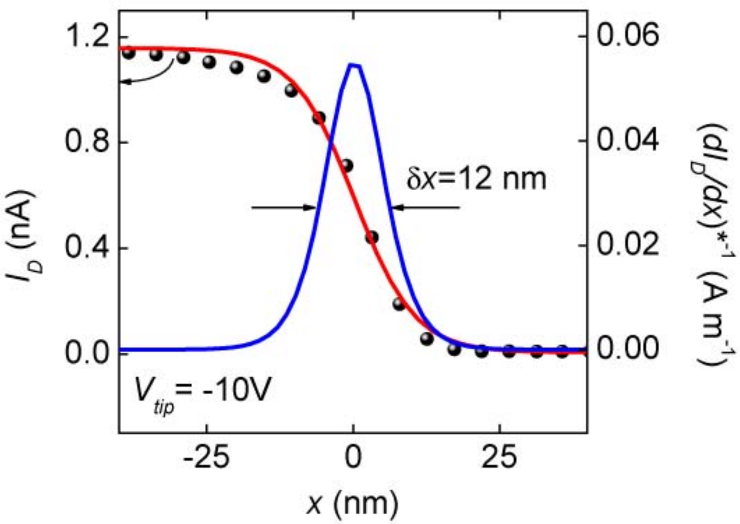
Erasing



C. Cen, S. Thiel, G. Hammerl, C. W. Schneider, K. E. Andersen, C. S. Hellberg, J. Mannhart, and J. Levy, *Nature Materials* *7, 298 (2008).*

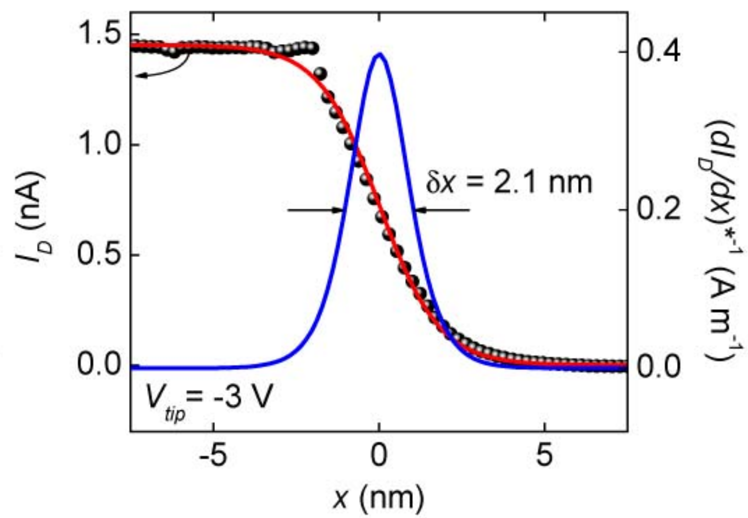
Ultranarrow Wires

V_{tip}=+10 V



12 nm

V_{tip}=+3 V

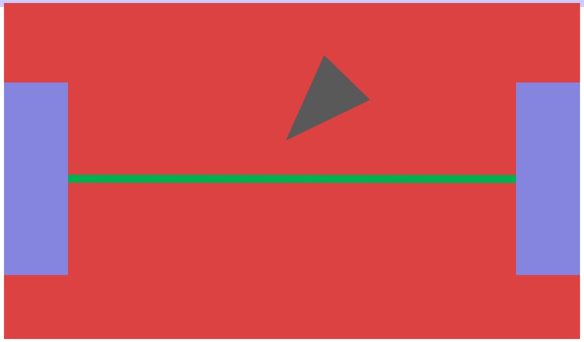


2 nm

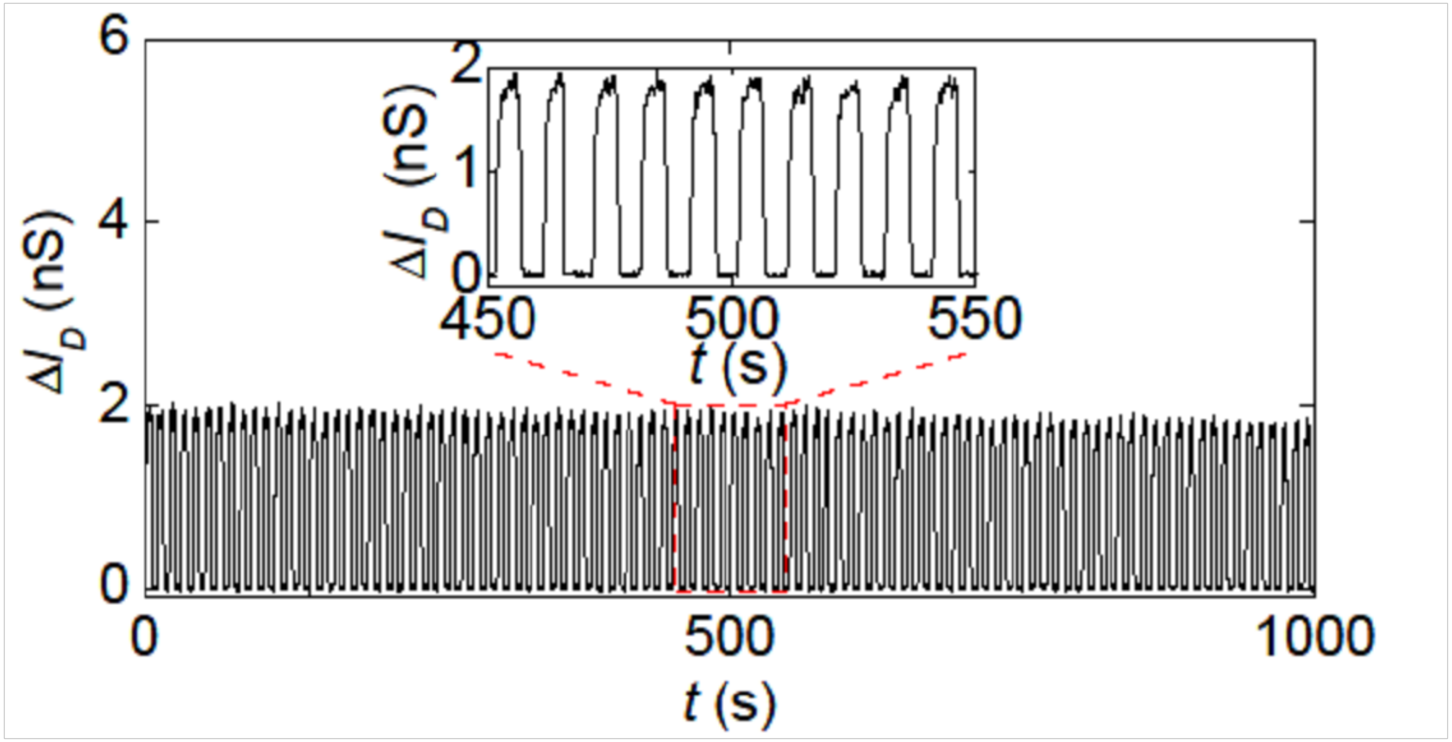
C. Cen, S. Thiel, J. Mannhart, and J. Levy, *Science* ***323****, 1026 (2009)*.

Multiple Write/Erase

Write with $V_{tip}>0$



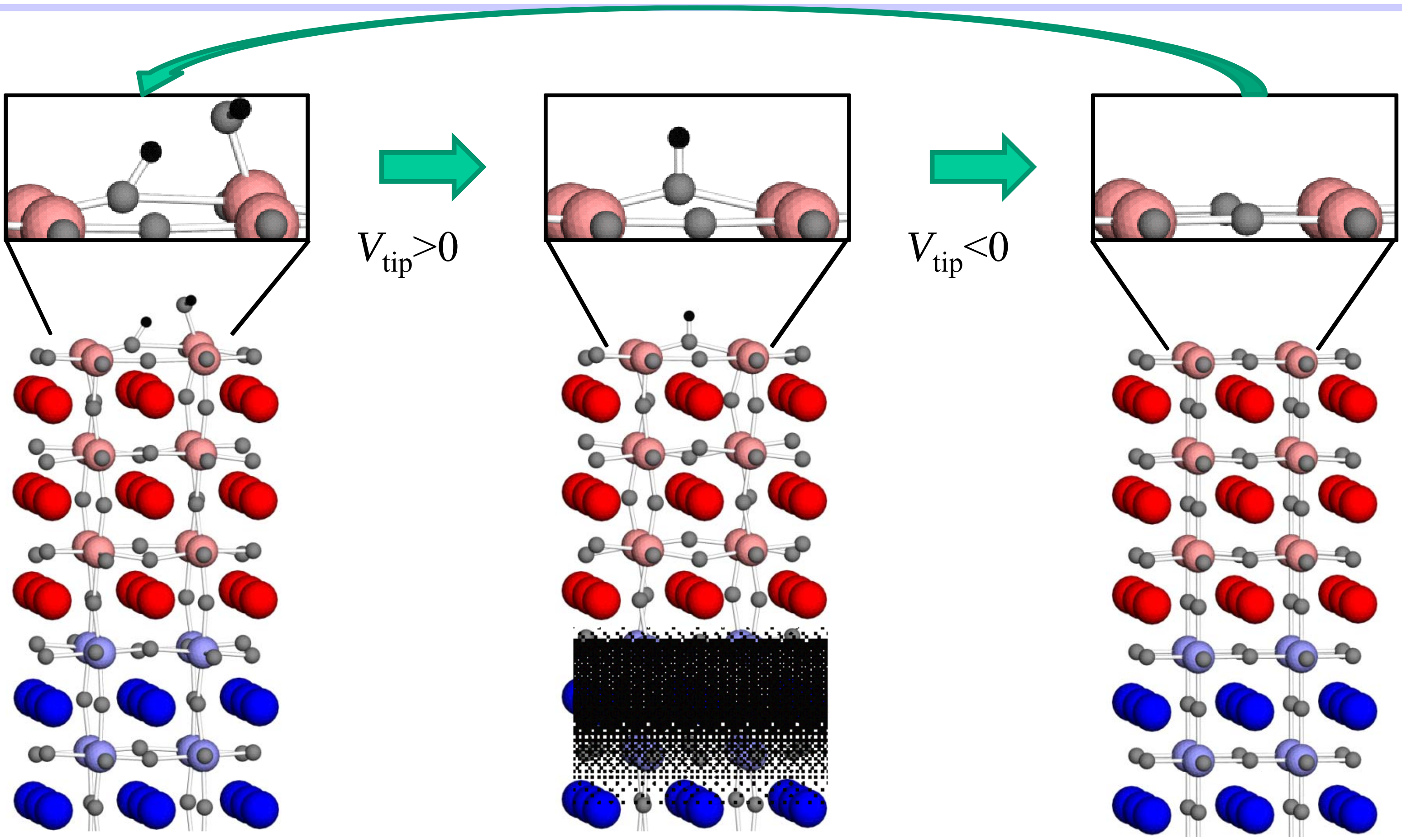
Erase with $V_{tip}<0$



C. Cen, S. Thiel, J. Mannhart, and J. Levy, *Science* ***323****, 1026 (2009).*

Possible Mechanism: “Water Cycle”

(C. S. Hellberg, unpublished)



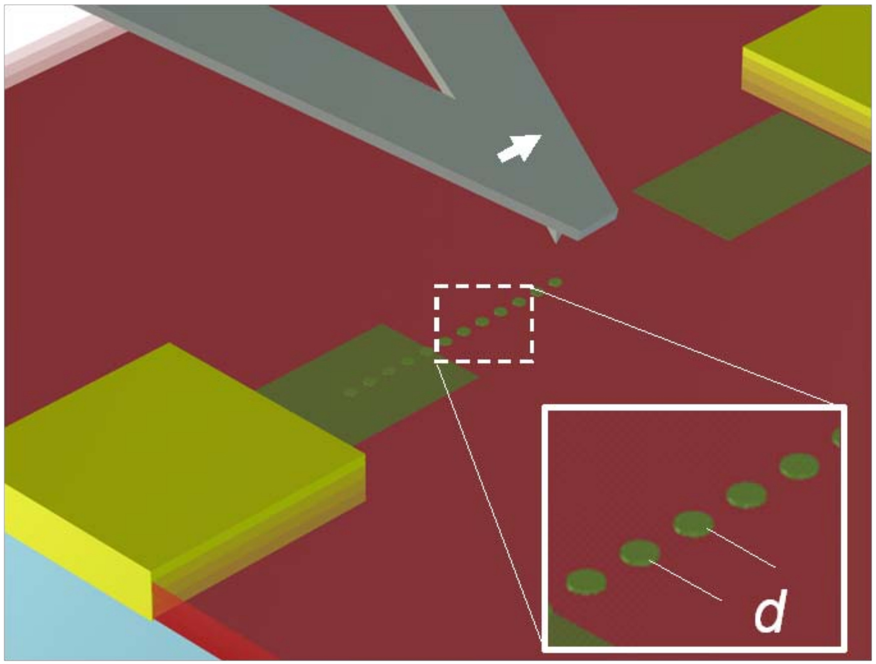
H_2O adsorbs, dissociates on $LaAlO_3$ surface

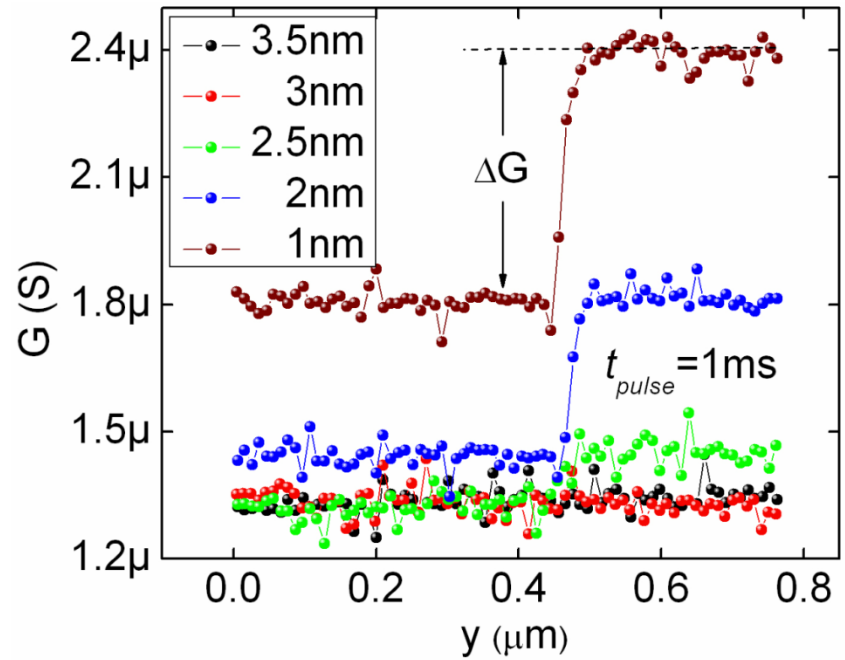
Positive tip removes OH-, leaving H^+ on surface and producing conducting interface

Positive tip removes H^+, restoring insulating state.

Ultrahigh Density Memory

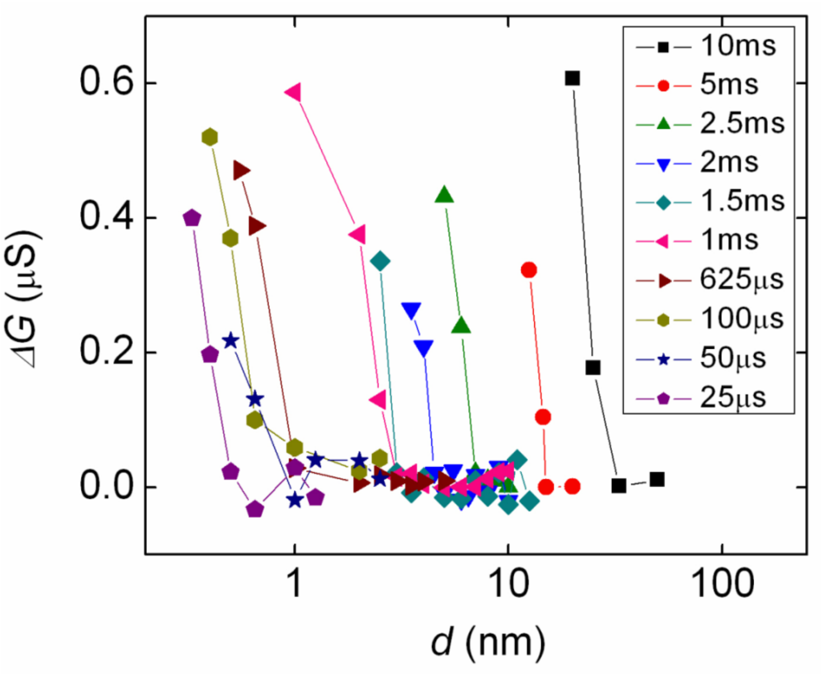
Density Limits for Isolated Dots

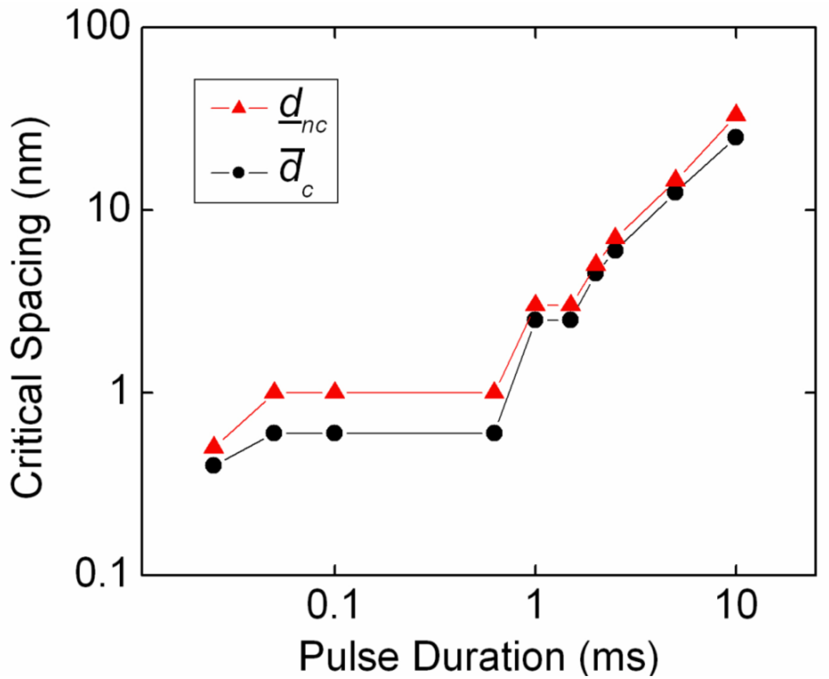




C. Cen, S. Thiel, G. Hammerl, C. W. Schneider, K. E. Andersen, C. S. Hellberg, J. Mannhart, and J. Levy, *Nature Materials* **7**, *298 (2008)*.

Density Limits for Isolated Dots

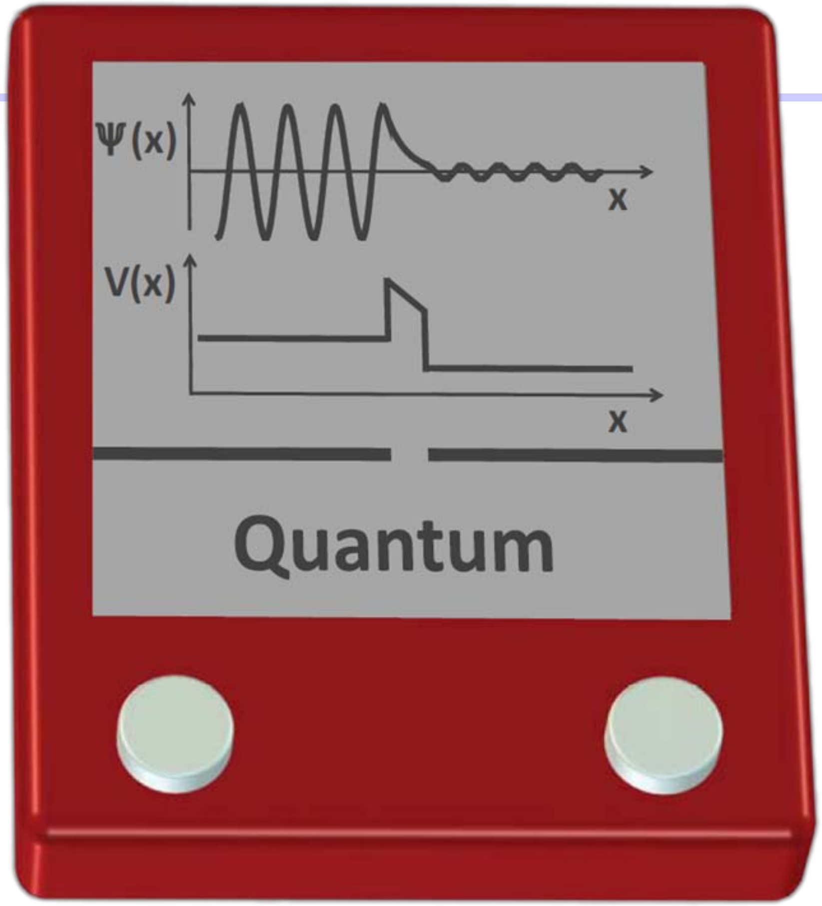




Smallest dot size ~1 nm

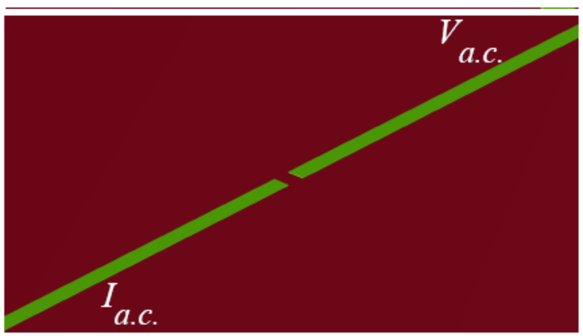
C. Cen, S. Thiel, G. Hammerl, C. W. Schneider, K. E. Andersen, C. S. Hellberg, J. Mannhart, and J. Levy, *Nature Materials* **7**, *298 (2008).*

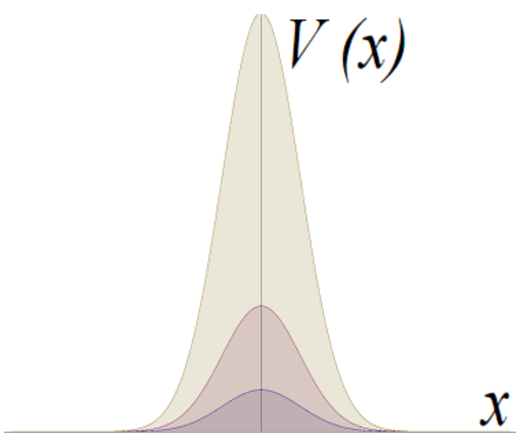
Quantum Mechanics On-The-Fly

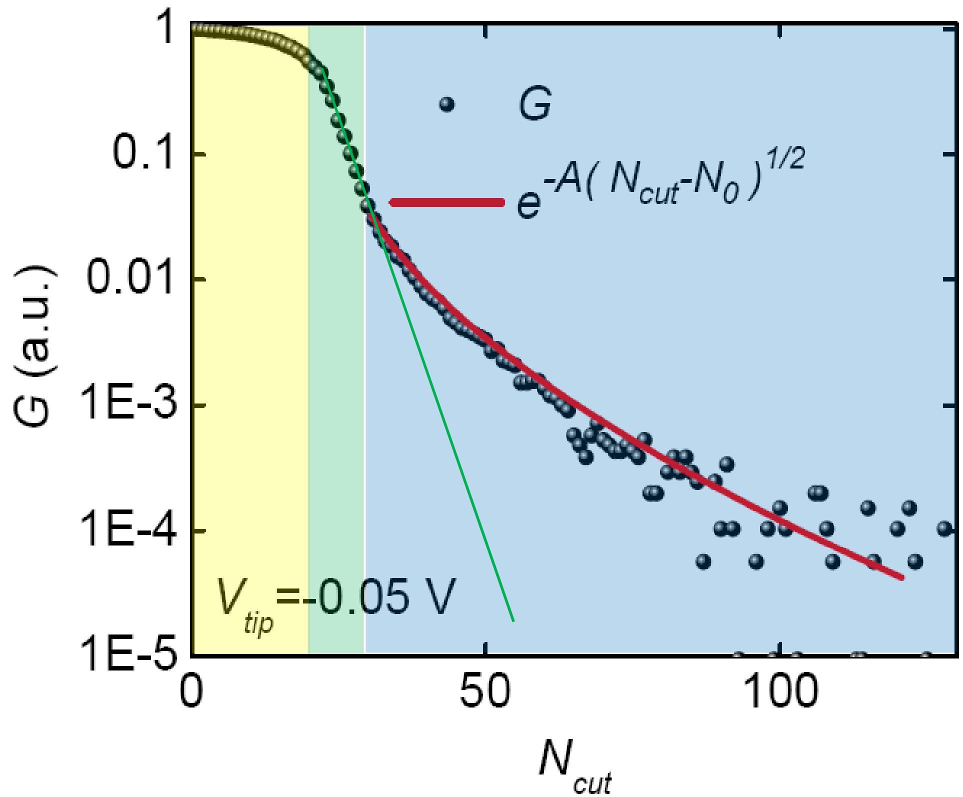


Designer Tunnel Barriers

- Transmission experiment
  - Three regimes observed



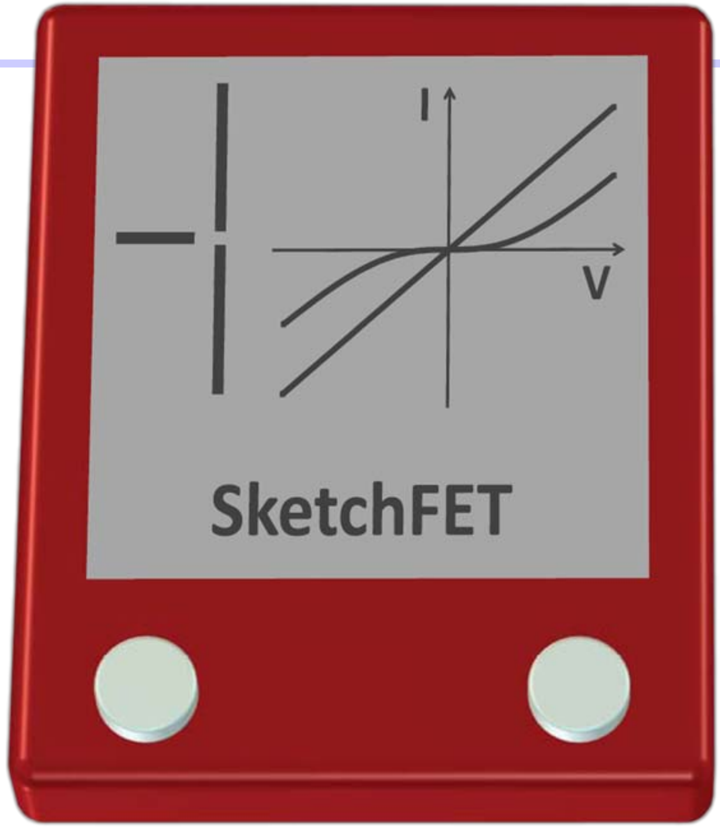




Conductive→ Hopping→ Tunneling

C. Cen, S. Thiel, J. Mannhart, and J. Levy, *Science* ***323****, 1026 (2009).*

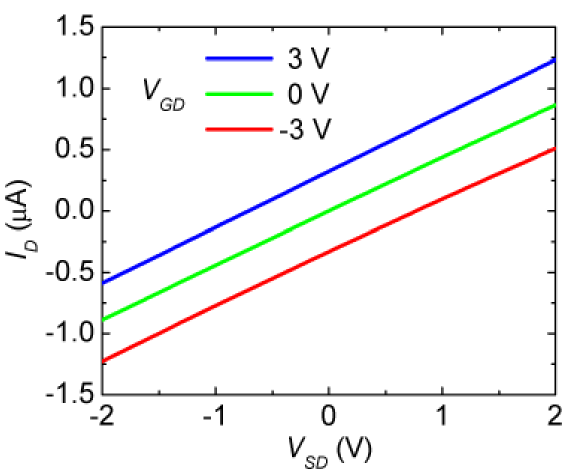
Transistor

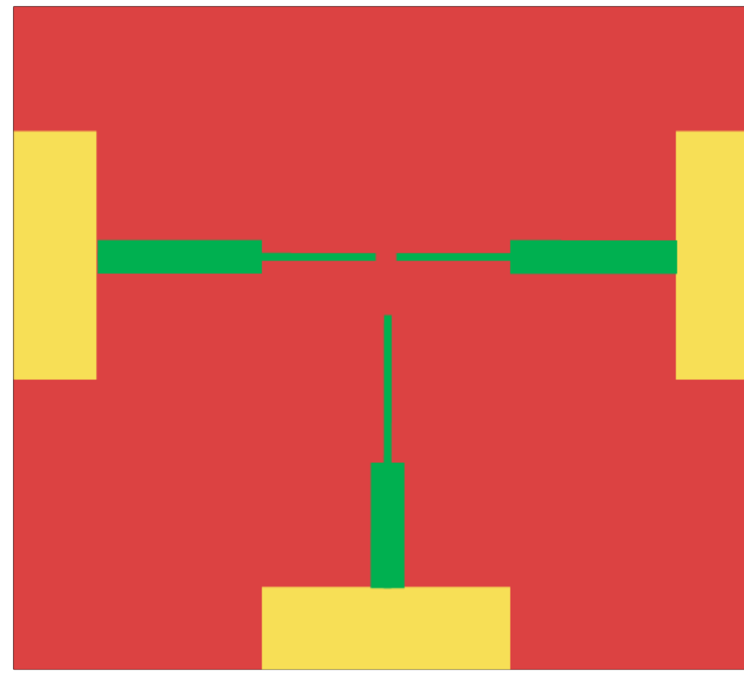


Sketch-based Electronic Transport within Complex-oxide Heterostructure Field-Effect Transistor

Creating a SketchFET

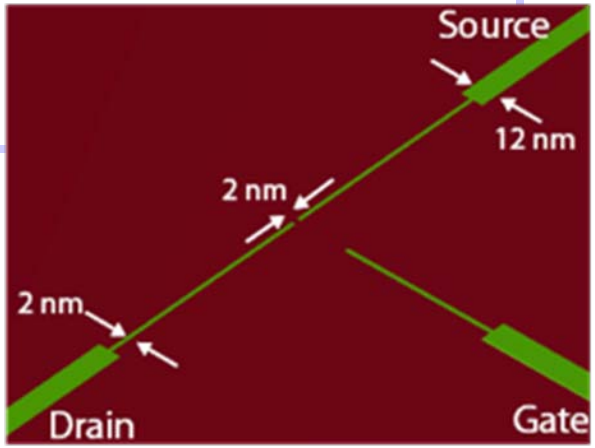
- Step 1
  - Write 12-nm (wide) T-junction
- Step 2
  - Erase 1 µm x 1 µm square
- Step 3
  - Write 2-nm T-junction
- Ste
  - C ... source a
- Ste
  - I ... e and s



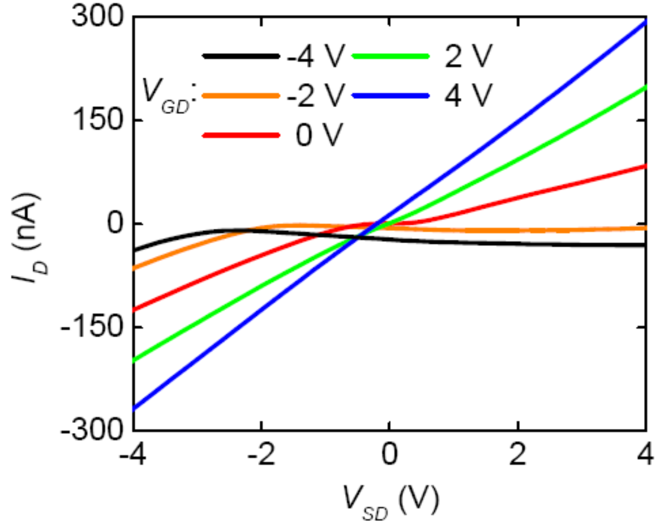


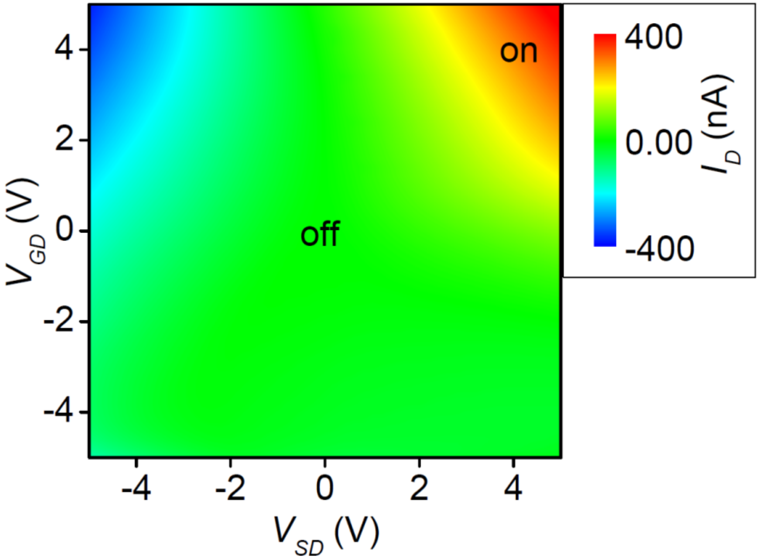
C. Cen, S. Thiel, J. Mannhart, and J. Levy, *Science* ***323***, *1026 (2009).*

SketchFET Properties



- Positive gate bias closes switch
- Negative bias opens switch
- No hysteresis observed
- Wider channel ←→ lower leakage





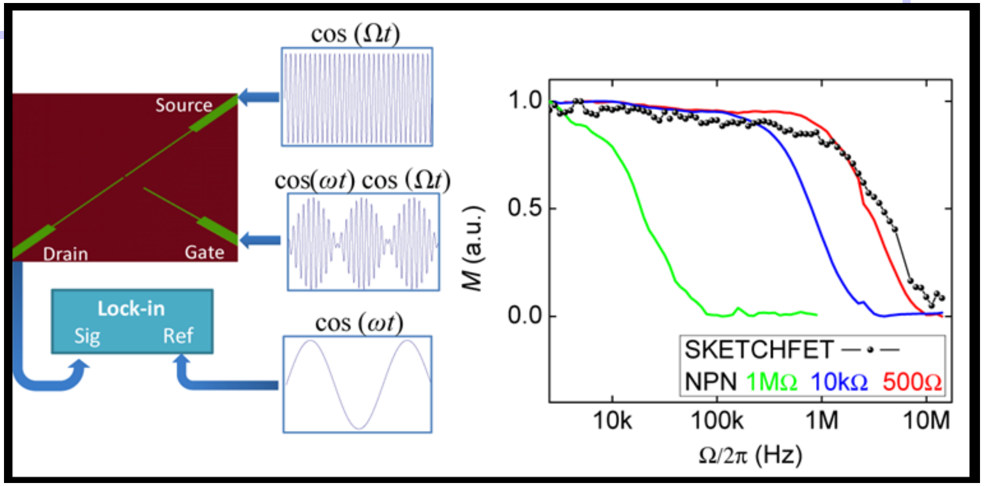
Can be used as an amplifier, switch or logic gate

C. Cen, S. Thiel, J. Mannhart, and J. Levy, *Science* ***323****, 1026 (2009).*

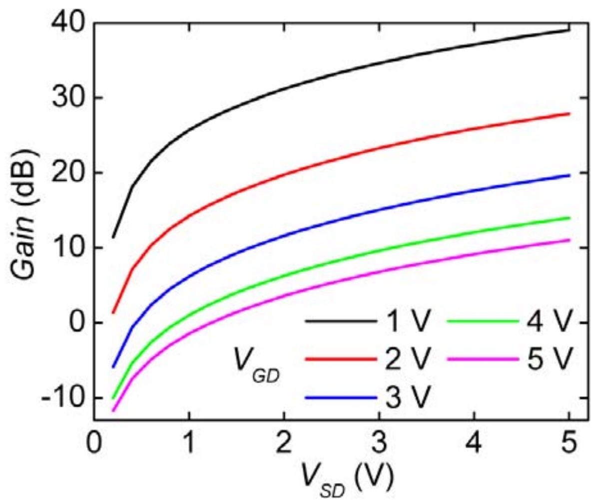
Summary for Room Temperature

- Near-atomic control over 2DEG top gate potential V(x,y)
  - Create quasi 0d,1d,2d structures with ease
  - Nonlinear functionality that could form the basis for "the next switch"
- Other facts
  - Can be grown on silicon
  - Optoelectronic devices

SketchFET Frequency Response



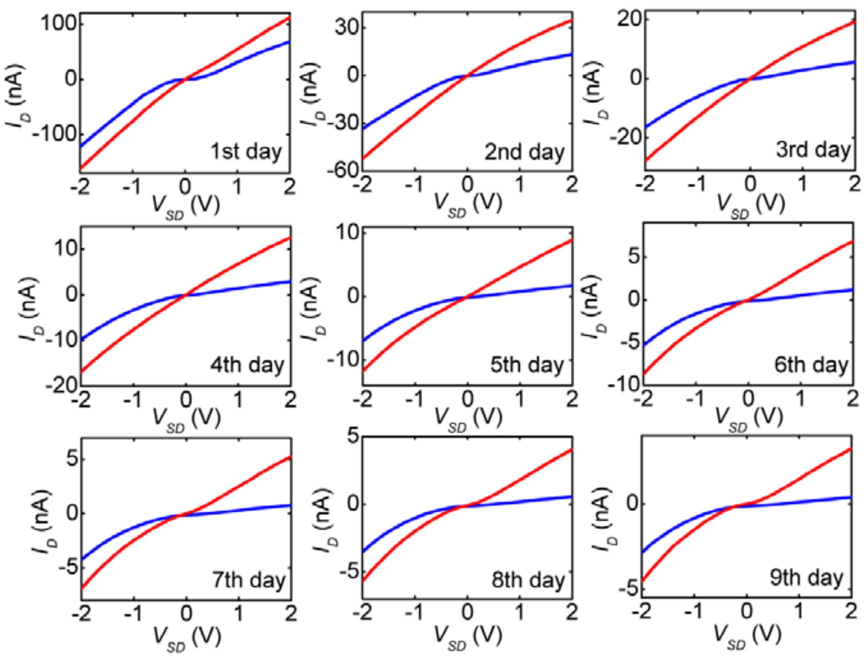
- Heterodyne experiment
  - use SketchFET as mixer
  - Compare with NPN BJT
- Measured cutoff frequency
  - ~ 10 MHz
  - Limited by ~MΩ lead resistance
  - Intrinsic value estimated to be ~ GHz
- SketchFET power gain
  - Up to 40 dB

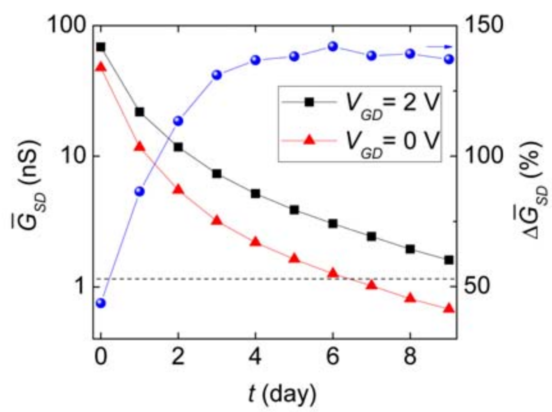


C. Cen, S. Thiel, J. Mannhart, and J. Levy, *Science* ***323****, 1026 (2009).*

Stability of Nanostructures

- Experiment performed at room temperature in vacuum (10^{-5} Torr)
- SketchFET figure of merit *increases*, then saturates
  - FOM=(G(2V)-G(0V))/ G(0V)
- Nanowire conductance drops toward planar value





C. Cen, S. Thiel, J. Mannhart, and J. Levy, *Science* ***323****, 1026 (2009).*

Future directions

Rewritable Memory and Logic

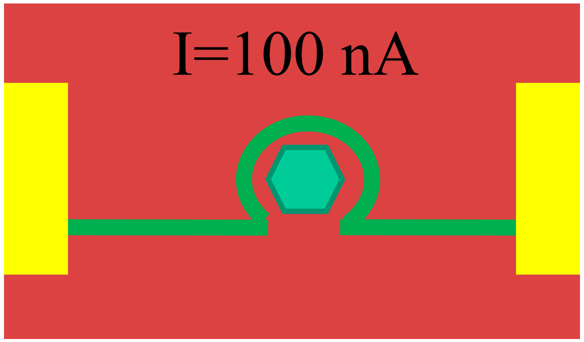
- Memory and logic traditionally made from different materials
- Transistors 1000x smaller than Penryn
  - Shrink facilities required to make circuitry by 10 orders of magnitude
    - FAB32 facility (3×10^6 m^3)
    - Ipod: ($\sim 10^{-4}$ m^3)
- Memory 1000x smaller than FLASH, magnetic storage
  - Millipede project ($\sim 10^3$ probes)

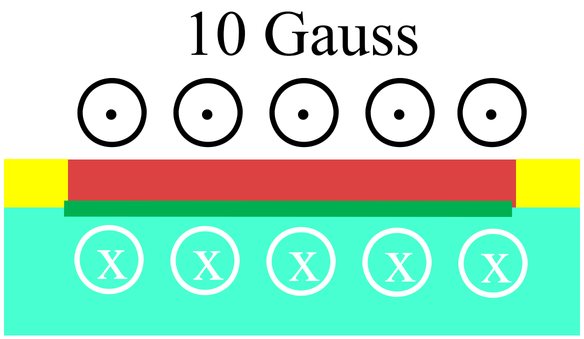
Low-Dimensional Transport

- Quantum Hall physics
- Coulomb blockade
- Resonant tunneling
- Single-electron transistor
- Anderson localization
- Luttinger liquid
- Nanoscale superconductivity

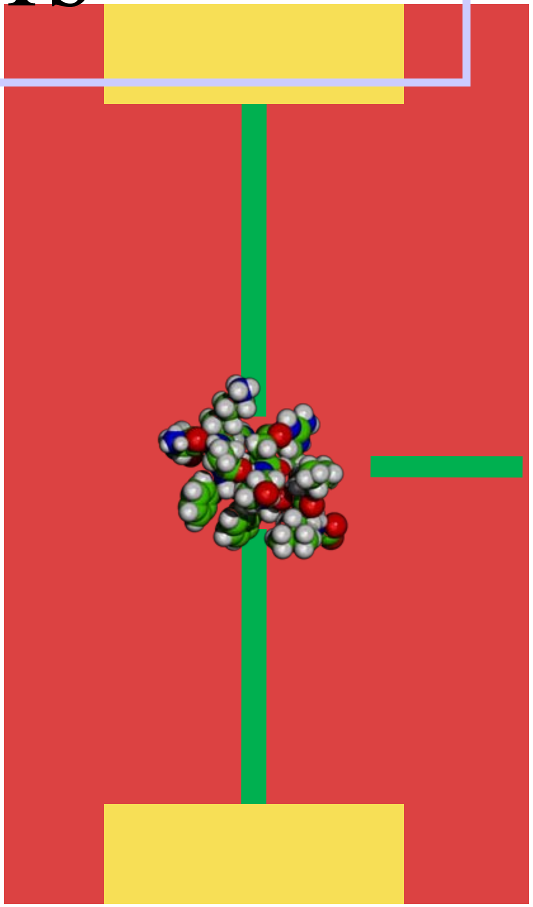
Nanoscale Magnetism and Spin Resonance

- Surface magnetic field
  - ~10 Gauss
- Excite and detect nearby magnetic nanostructures
  - Write inductor loops around magnetic samples
- Electron/nuclear spin resonance
  - Use SketchFET pre-amplifiers





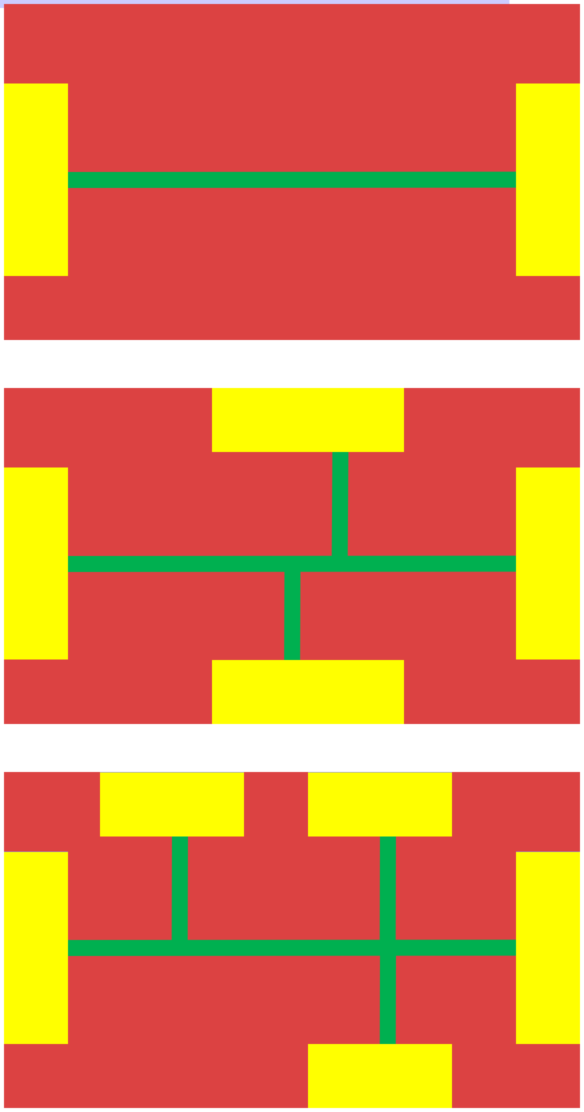
Nanoscale Sensors



- SketchFET channel sensitive to charge/oxidation state
  - Active area <5 nm^2
  - On-the-fly location
- Applications in biological and chemical sensing

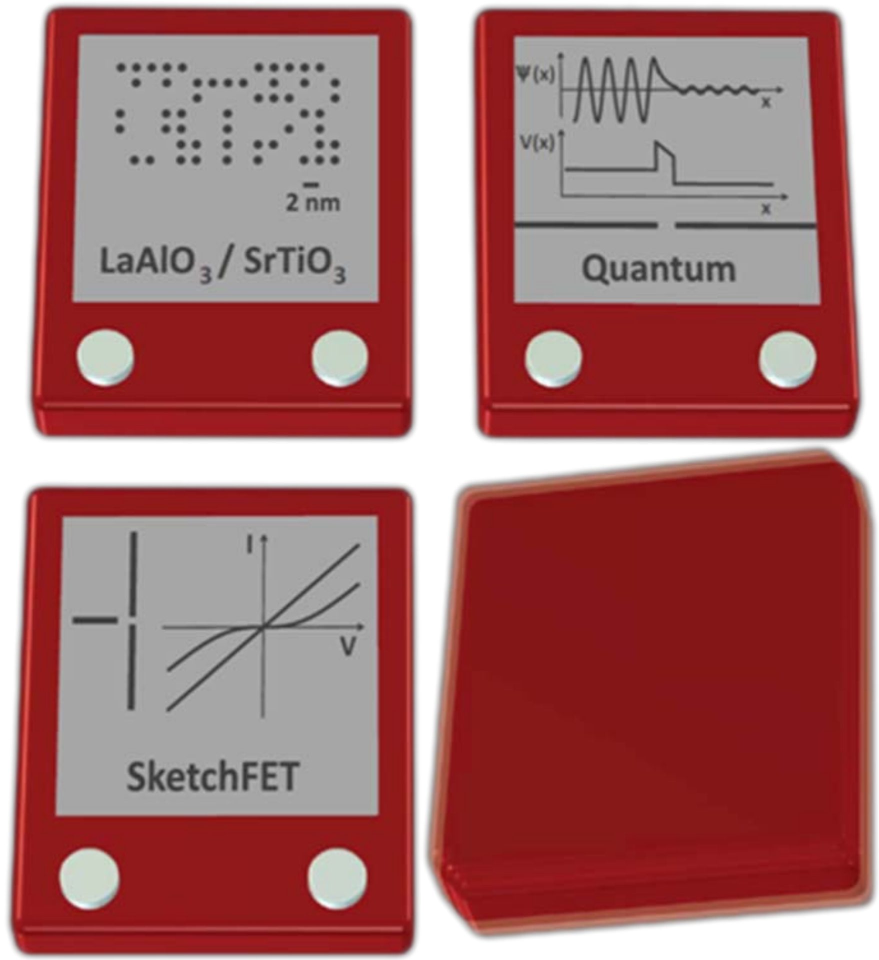
Self-Referential Measurements

- Nanowire measures 2DEG thickness
  - Comparable to nanowire width
- Four probe measures conductivity
- Double-junction expts reveal in-plane modulation doping
- Five probe measures Hall mobility



Summary

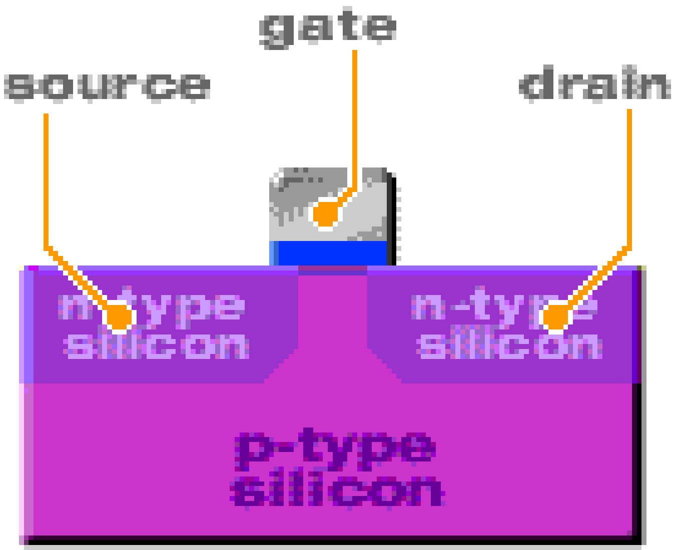
- Oxide Nanoelectronics Platform
  - Ultra-high-density memory
  - Control over tunnel barriers
  - SketchFET
- Possible applications
  - More Moore
    - Scaling far beyond CMOS, magnetic recording
  - Much More than Moore
    - Integrated, reconfigurable logic + memory
    - Biosensing applications (SketchFET)
    - Magnetic sensing
    - Quantum simulations
    - Superconducting nanostructures
    - Topological quantum computing
    - …



Transistors

A device composed of semiconductor material that amplifies a signal or opens or closes a circuit. Invented in 1947 at Bell Labs, transistors have become the key ingredient of all digital circuits, including computers. Today's microprocessors contains tens of millions of microscopic transistors.

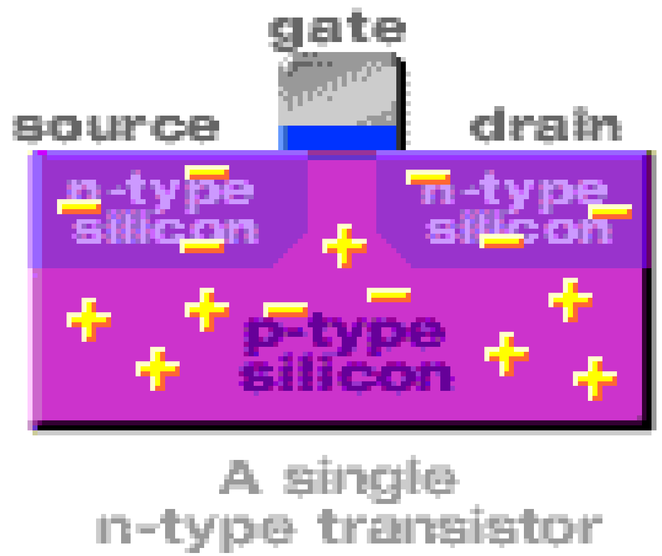
Transistors



A single
n-type transistor

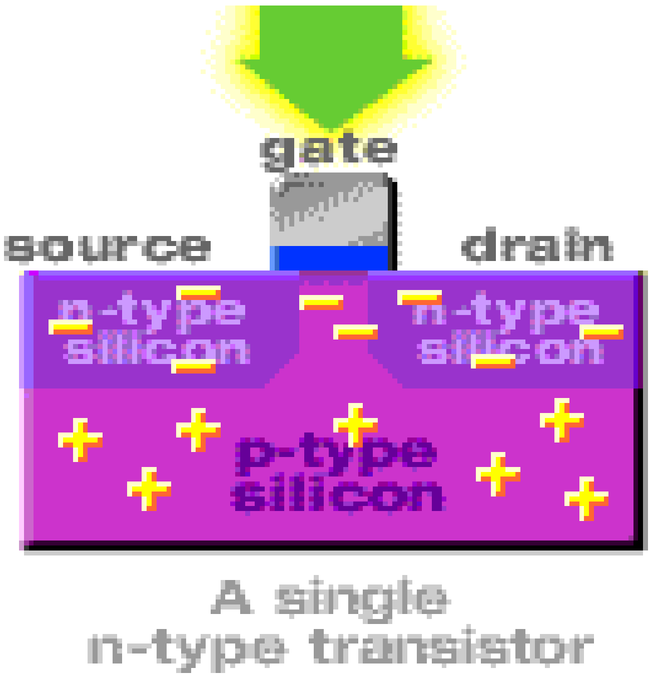
Transistors consist of three terminals; the source, the gate, and the drain.

Transistors



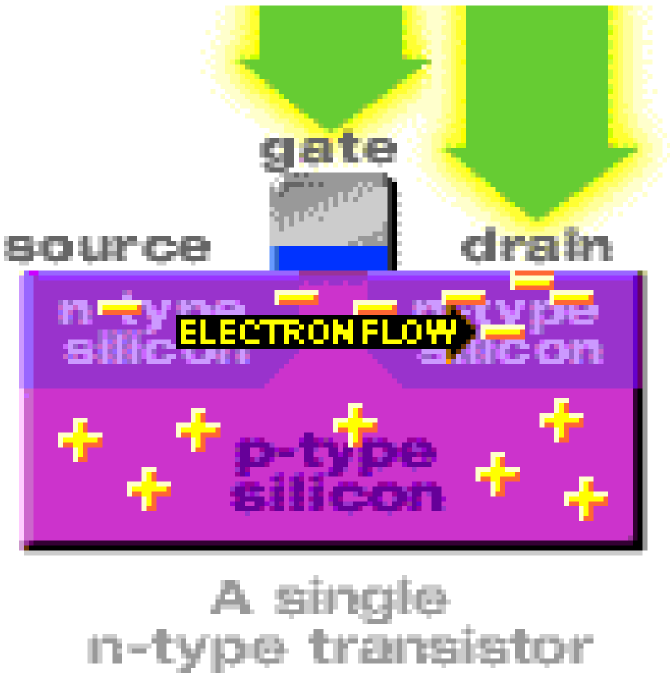
In the n-type transistor, both the source and the drain are negatively-charged and sit on a positively-charged well of p-silicon.

Transistors



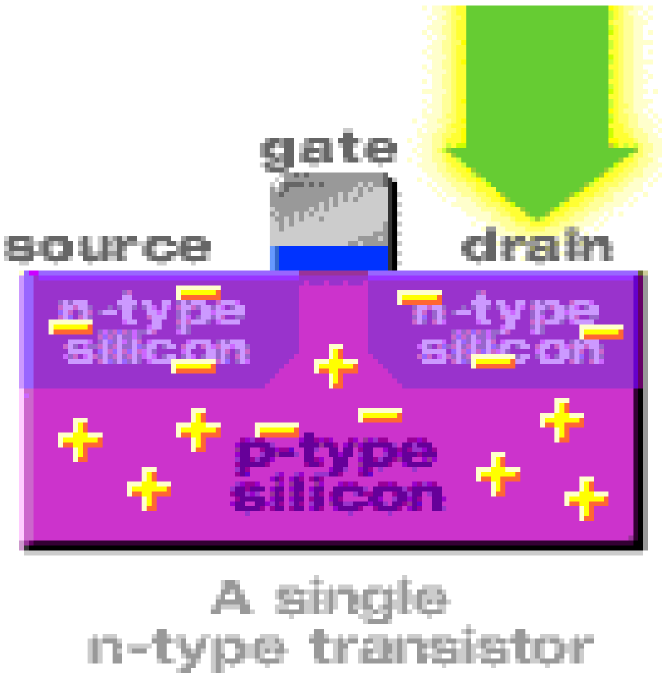
When positive voltage is applied to the gate, electrons in the p-silicon are attracted to the area under the gate forming an electron channel between the source and the drain.

Transistors



When positive voltage is applied to the drain, the electrons are pulled from the source to the drain. In this state the transistor is on.

Transistors



If the voltage at the gate is removed, electrons aren't attracted to the area between the source and drain. The pathway is broken and the transistor is turned off.

Nanoscale Electronics

- Since it's invention in 1947, the transistor has continually shrunk over the years according to a prediction by Gordon Moore, who stated that the number of transistors on a chip would double every 18 months.
- Unfortunately, as we will see today, this trend is predicted by many to end within the next 10 – 15 years due mainly to the changing physics of devices scaled below 0.10 microns (100 nm).

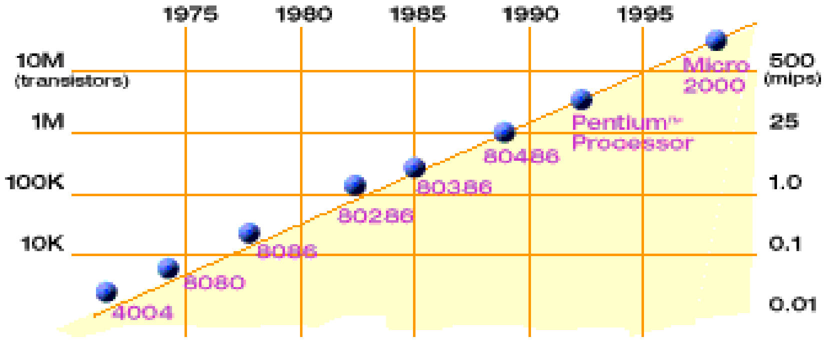


Figure 1

Image courtesy of Intel Corp.

- Nanoscale Devices: Electronic devices that are designed with lateral features of 100 nm or less. Designers began searching for a new name for their smaller devices for two main reasons:
- Fabrication Difficulties
- Physical Operation: Bulk Properties of Physics VS. Quantum Mechanics

(An overview of both will be covered soon!)

- To understand the problem, let's review the operation of the most popular transistor in use today, the MOSFET (**M**etal-**O**xide-**S**emiconductor **F**ield **E**ffect **T**ransistor)

- MOSFETS are built starting with a substrate that is doped, or loaded with impurities that give the substrate a large amount of extra mobile charge (positive in the case of holes, negative in the case of electrons.)

MOSFET Operation Animation

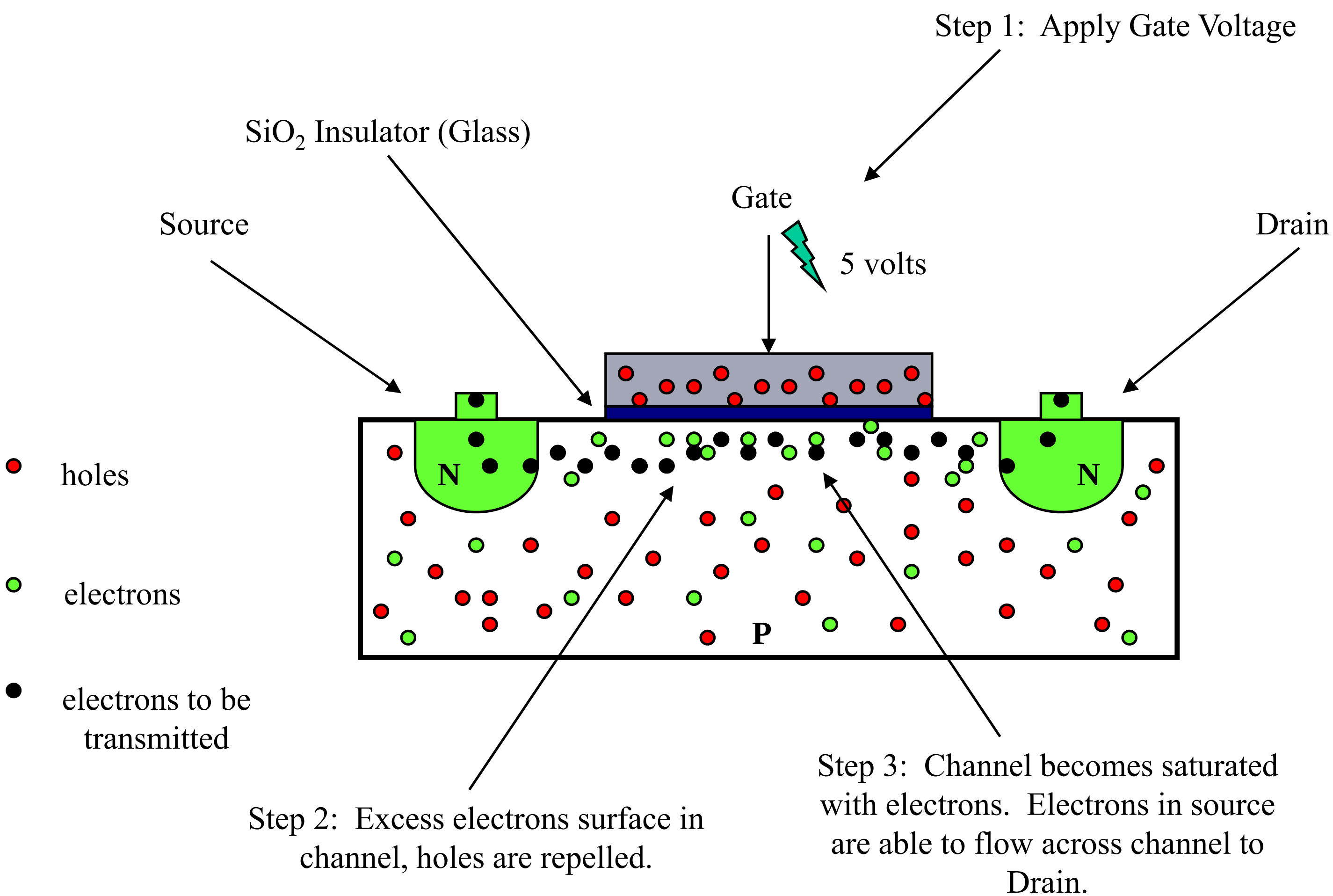


Figure 2

Image courtesy of me. =o)

MOSFET Fabrication Problems

- Present Day Fabrication Method (Lithography): IC Pattern is projected in 1 cm^2 increments onto a silicon wafer using UV light and a series of lenses that reduce the pattern to some given required resolution. Each 1 cm^2 section contains roughly 10^9 picture elements (pixels).

- Nanoscale Devices: Most features of the typical nanoscale device are too small to be made like present day devices so a sharp focused beam of electrons is used to build the 1 cm2 pattern one device at a time. Of course, this is way too slow for mass fabrication.

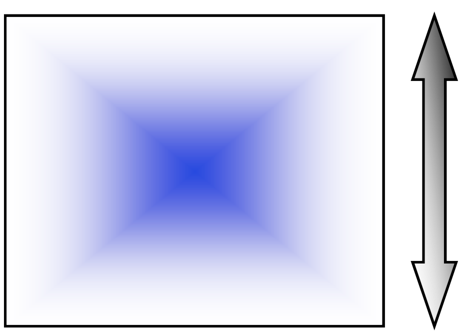
Quantum Mechanics Review

- Wave-like characteristics of charge carriers are present at both small and large scale (read: nanoscale and 0.10 micron and above) levels, but we have usually neglected the wave-like nature of carriers in favor of the classical bulk properties carriers exhibit when observed in devices with smallest dimensions above 100 nm.

- As device parameters shrink well below this value, quantum mechanics comes into play and the wavelength (= h/p) of the electron can no longer be ignored.

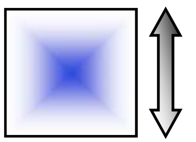
Particle-in-a-box Example

Classical (Big)



Continuous Particle Energy Levels

Quantum (Small)



Only discrete particle energy levels (less as the box shrinks!)

F
A
B
R
I
C
A
T
I
O
N

Difficulties in CMOS Scaling[2] below 0.10 μm

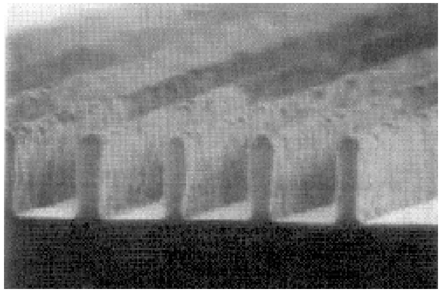


Figure 3 - X-RAY Lithography – 80 nm wide lines.[2]

- As mentioned earlier, CMOS devices are currently fabricated using some form of lithography. In order to obtain the minute resolution needed for the nanoscale regime, optical lithography (using a 193 nm wavelength laser) with phase-shifting could be used. Unfortunately, this method relies on surface changes in the mask that cause interference patterns that sharpen the image cast on the silicon. Due to this geometric dependence, this method is not very useful for building arbitrary devices. (.10 to .12 μm)

- X-Ray Lithography is another possible solution to the fabrication problem. In this method, an x-ray emitting device is passed over (very closely) silicon covered in an x-ray absorbing material (such as Au) to image a circuit. The problem with this mainly is that the absorbing material cannot be pressure-deformed as this will alter the image accuracy. (30 nm features)

- Electron Beam (Projection Lithography): Two different methods using similar technology. Main difficulties here are throughput and Coulomb interactions and geometric imperfections. (10 nm and 50 nm respectively)

P
O
W
E
R

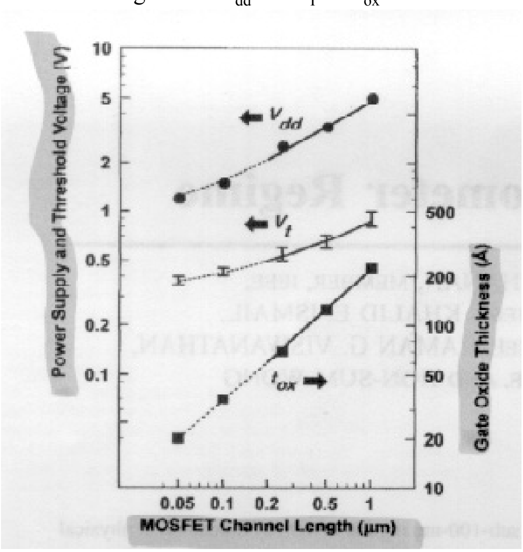
A
N
D

V_T

$$P_{ac} = (C_{sw} V_{dd}^2/2)f$$

- As CMOS get smaller, active power and electric field become more of a concern to designers. To curb active power consumption, source voltage is scaled at a cost of gate delay.
- Figure 4 – $P_{off} = W_{tot}V_{dd}I_{off} = W_{tot}V_{dd}I_0\exp(-qV_{t,wc}/mkT)$

Figure 4 – V_{dd} vs. V_T vs. t_{ox}[2c]



In essence, V_T does not scale much since the inverse subthreshold slope (which represents transistor turn-off rate) is dominated by temperature, not V_T or V_{dd}. Also, V_T must be around 0.3V-0.4V (or leakage current causes high standby power). Thus, increasing V_T/V_{dd} above 0.3 results in large CMOS delay. (One way to deal with this would be to use two types of transistors, one with a small V_T, the other large.)

Short channel effect also help determine V_{Tmin}.

S
H
O
R
T

C
H
A
N
N
E

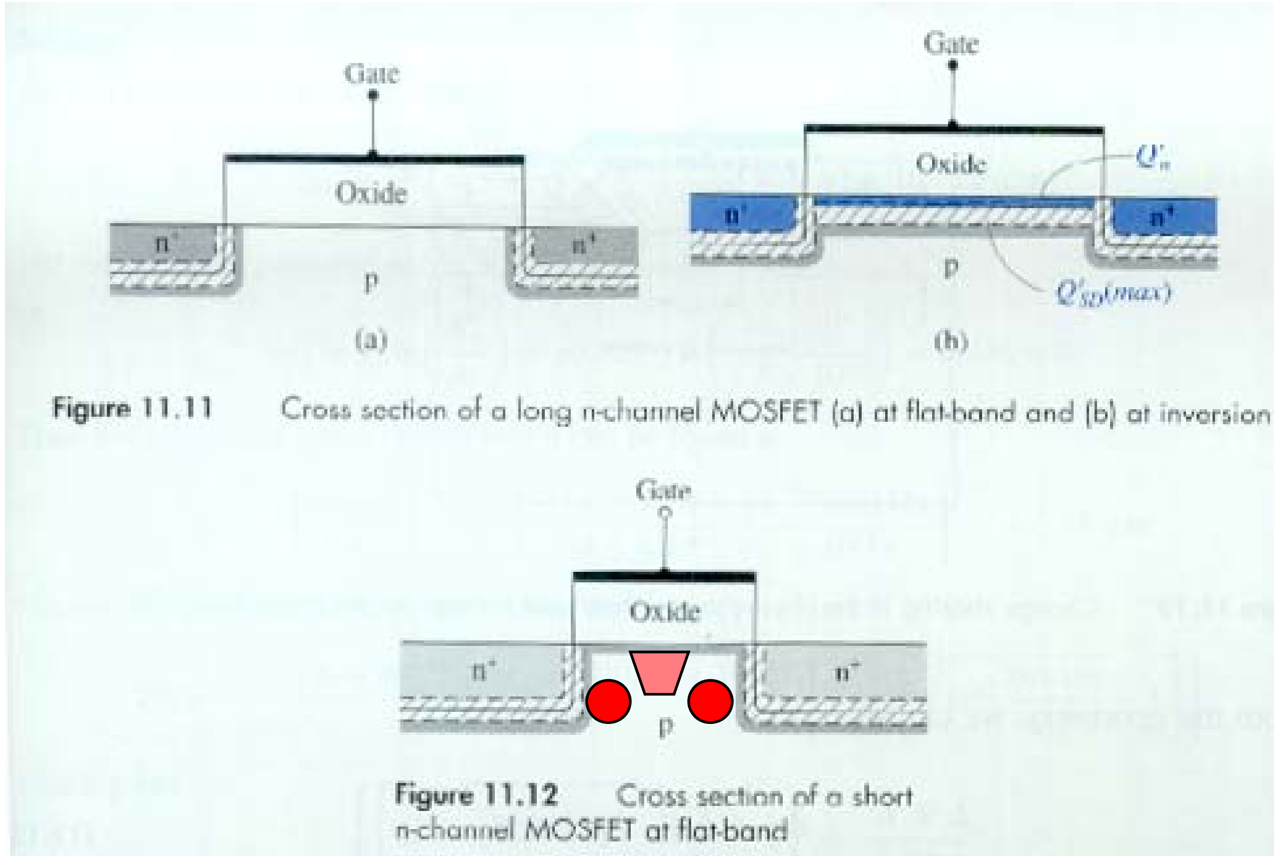


Figure 5 – Illustration of the short-channel effect.[3]

Short-Channel Effect: As channel length decreases, space charge regions at the source and drain encroach on areas normally controlled wholly by the gate. To defeat this effect, some designers have employed non-uniform channel doping procedures. Unfortunately, no mention was made on the accuracy of this method.

G

A

T

E

O

X

I

D

E

- In order to keep V_T variations under control when dealing with short-channel effects, the gate oxide thickness is reduced. Eventually this leads to quantum tunneling of electrons from the gate to the silicon substrate which results in leakage current.
- Given different oxide thickness, the authors of (2) have shown that the minimum acceptable leakage current for a device with V_{dd} = 1V is roughly 1A/cm^2. This corresponds to an oxide thickness of roughly 20 Å.
- Unless a new gate dielectric is developed, leakage current due to tunneling will force minimum transistor dimensions (ie. channel length) to be 25-50 nm.
- Another problem with a thin gate oxide is loss of inversion charge. This is due to polysilicon gate depletion and inversion layer quantization effects.

Summary of CMOS Scaling Difficulties

- Mass Fabrication is a problem as well as accuracy and resolution for varying geometries.
- Power fluctuation and varying threshold voltage cause unacceptable power consumption.
- Short channel effect decreases the gate's ability to control the depletion region and allow current to flow as it normally would with a long channel length.
- As the gate oxide thins, electrons can tunnel from the gate to the silicon substrate which results in leakage current.

Question: Can we come up with an alternate solution to the CMOS scaling problem?

Possible Solution: Resonant Tunneling Devices

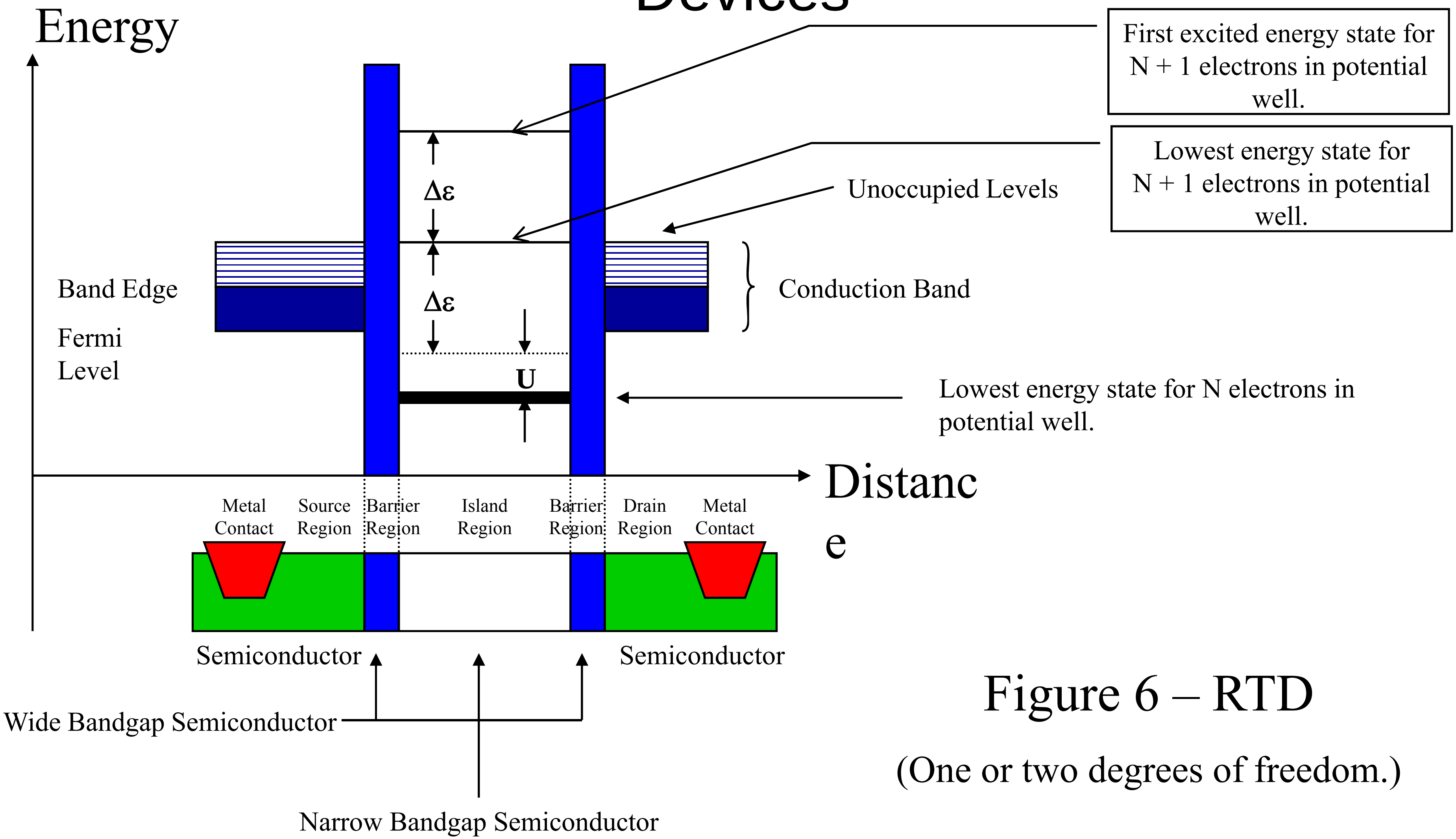


Figure 6 – RTD

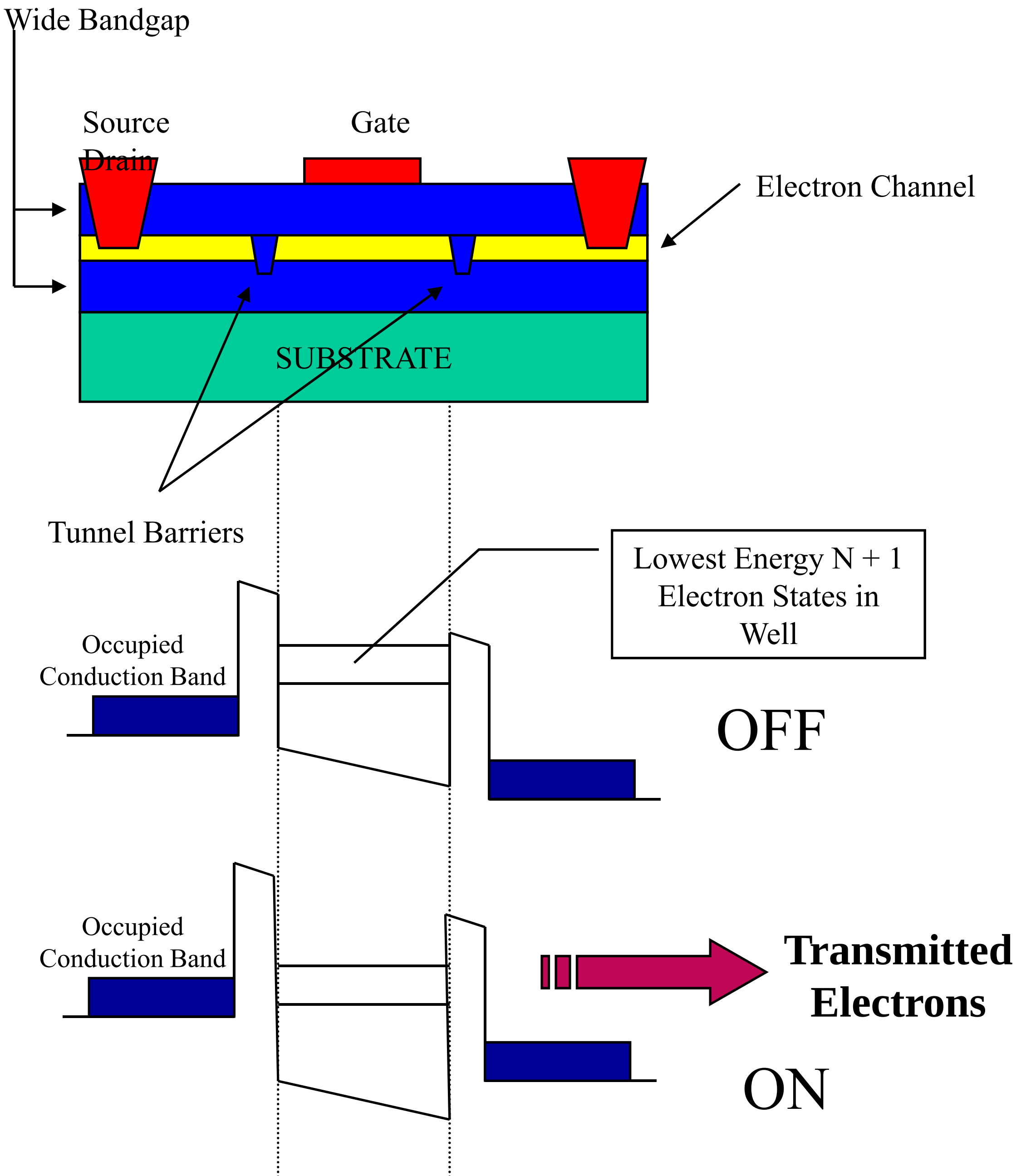
(One or two degrees of freedom.)

- Quantum mechanics requires that each electron's energy level be quantized. There are a finite number of such levels and as the barriers of the island encroach on the island itself, the separation of energy levels grows. In other words, $\Delta\varepsilon$ increases. (U is the "repulsion energy electrons must overcome to get on the island.)

- Also dictated by quantum mechanics is electron tunneling: If the barriers are thin enough an electron with energy lower than that of the height of the barrier could tunnel through the barrier so long as there is an empty state of the same energy level waiting on the other side.

- A bias potential can be applied from the source to drain to incite electron movement. This condition occurs only when the bias potential is sufficient enough to lower the energy of an unoccupied one-electron state on the island so that it is in the range of the conduction band of the source. The well is then "in resonance."

Resonant Tunneling Transistor



- A bias voltage applied to the gate lowers the energy of all the states in the well, bringing them into resonance with the mobile electrons in the occupied conduction band of the source.
- There are other, more complicated details at work (ie. Multiple on and off states, 3-dimensional considerations, etc) that will not be covered here.

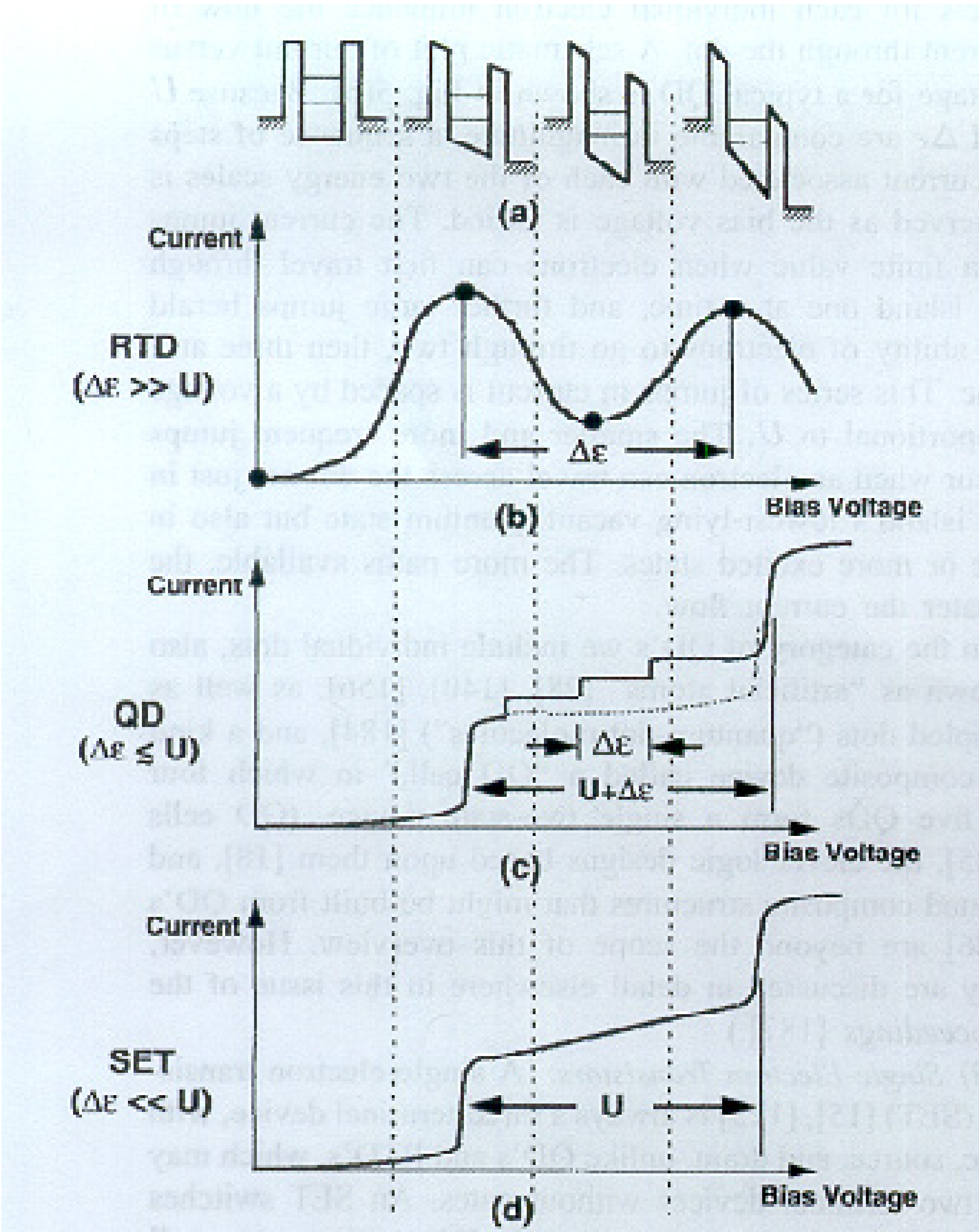
Figure 7 – RTT

(One or two degrees of freedom.)

Single Electron Transistor

(Three degrees of freedom.)

- Similar to RTD's except SET's are three terminal devices and their islands are generally made of metal, not silicon. (Incidentally, having a metal island causes an emphasis of U over $\Delta\varepsilon$.)
- A significant voltage on the gate causes a single electron to tunnel onto the island, but Coulomb blockade causes it to tunnel to the drain just as quickly. This happens over and over as long as the gate voltage is not increased further. A "one electron excess" equilibrium of sorts occurs and current stops flowing just as quickly as it started.



Resonance
Blending

$\Delta\varepsilon > E_F - E_{Band}$

Figure 8 – Current VS. Bias Voltage.[1]

Electron
Accumulation

Nanoscale Electronics: The Good, The Bad, The Ugly

- The Good:
  - Multiple “on states” adds functionality to nanoscale devices, which could reduce area per function, which would in turn reduce the temperature dissipation problem.
  - Bulk physical properties that FET’s rely on disappear around 100 nm. Nanoscale devices capitalize on this very obstacle to further miniaturization of FET’s.
  - Doped materials are no longer necessary.

- The Bad:
  - Valley current: Even when out of resonance, devices do not completely shut off. Two possible problems are inherent here: first, power could be an issue and second, on and off states may not be distinguishable when working with different devices in a chip.
  - Nanoscale devices only operate at very cold temperatures (cryogenic.) At room temperature, random thermal motion gives electrons the extra “boost” they need to tunnel. (However, this can be overcome by a careful choice of island dimensions to control U and $\Delta\varepsilon$.
  - Fabrication is again a problem because barriers need constant thickness, and the very nature of the devices demands precision.

- The Ugly:

There really isn’t an “Ugly” category, but I couldn’t very well leave it out.

Reference Listing

1. Goldhaber-Gordon, et. al., “Overview of Nanoelectronic Devices.” Proceedings of the IEEE, Vol. 85, NO. 4, April 1997.

2. Taur, Yuan, et. al., “CMOS Scaling into the Nanometer Regime.” Proceedings of the IEEE, Vol. 85, NO. 4, April 1997.

3. Neamen, Donald A., “Semiconductor Physics & Devices.” ©1997 McGraw- Hill Companies, 2nd Ed., p. 501.

There is ***still plenty of room*** at ***the bottom***….