NTU lecture 070501

Advanced Device Fabrication Techniques

ChiiDong Chen 陳啟東

Institute of Physics, Academia Sinica

e-mail: chiidong@phys.sinica.edu.tw
url: www.phys.sinica.edu.tw/~quela

Outline:

1 State-of-the-art device fabrication techniques

Future light sources: EUV and e-beam

2 e-beam lithography

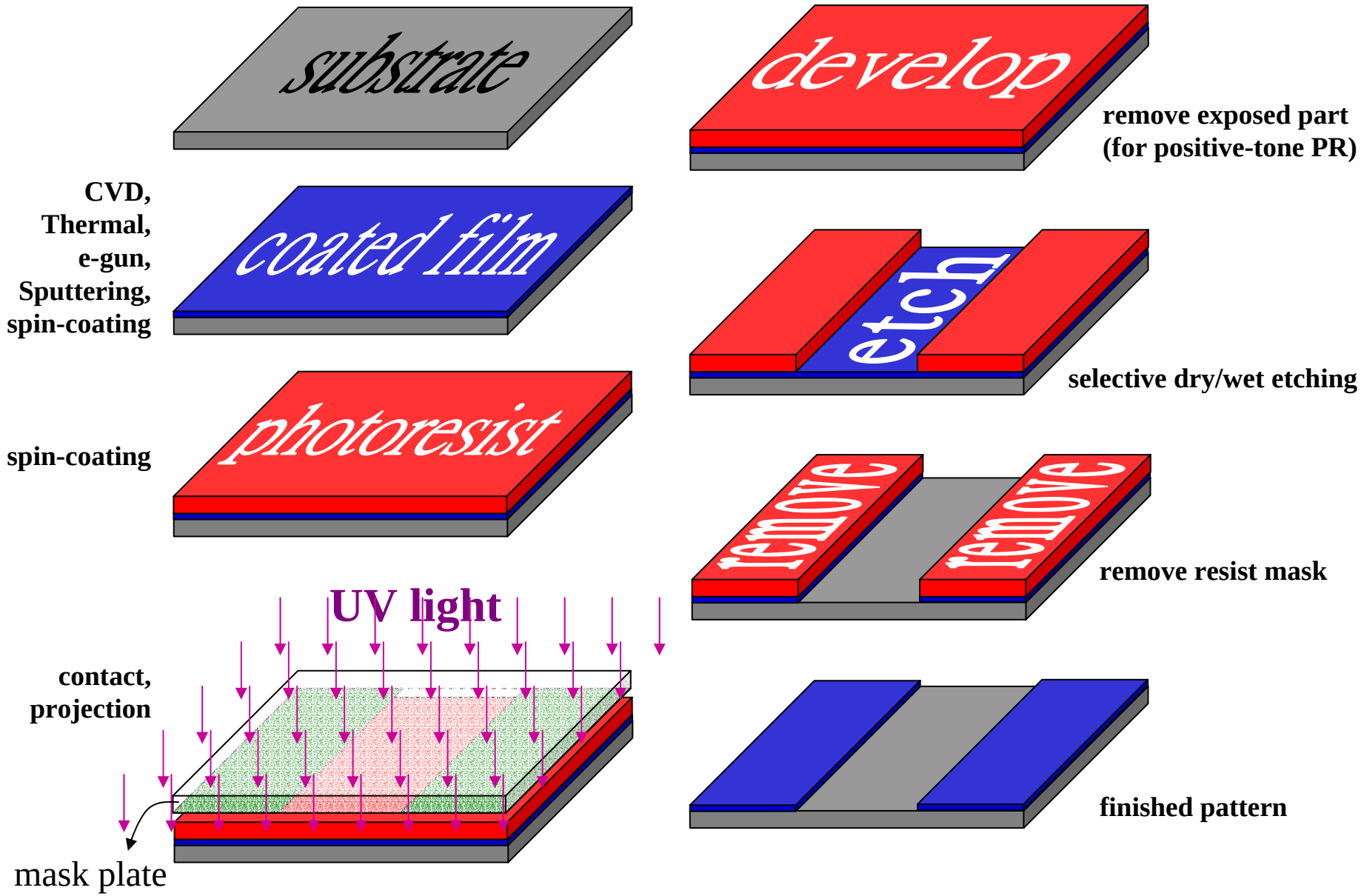
3 Examples:

nano-pore based point contact devices

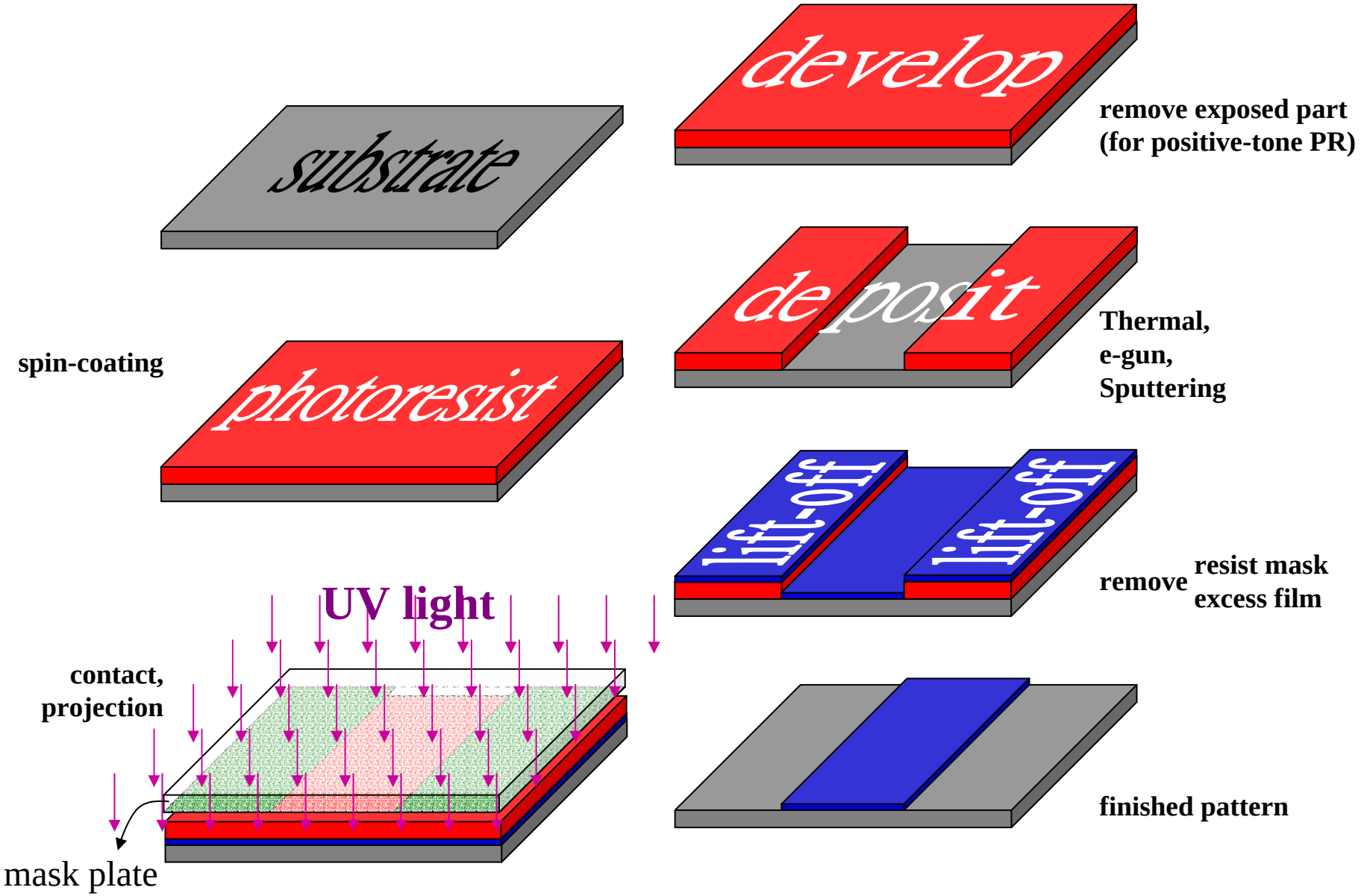
nano electronic devices

Lithography = Pattern transferring

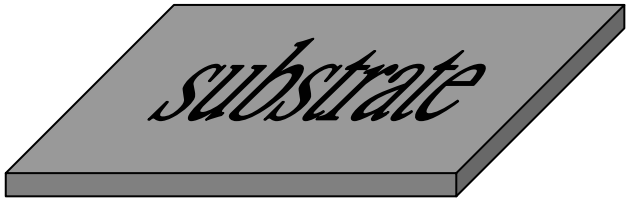
Standard etching process

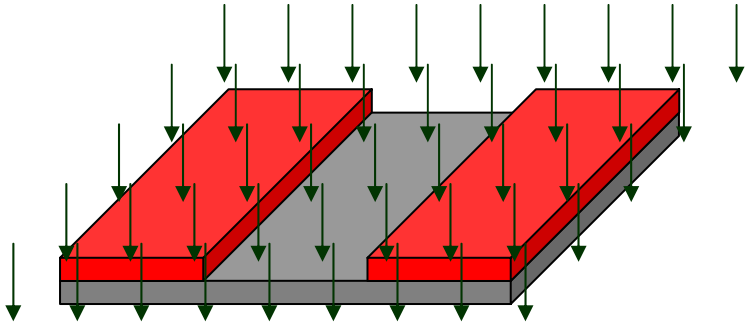


Complementary process: lift-off



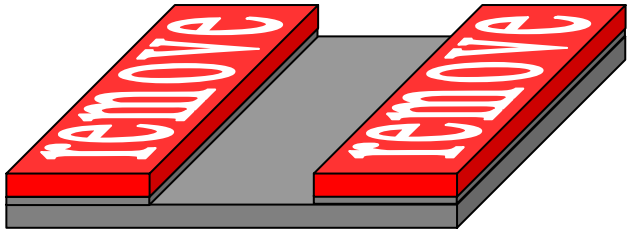
Substrate treatment process



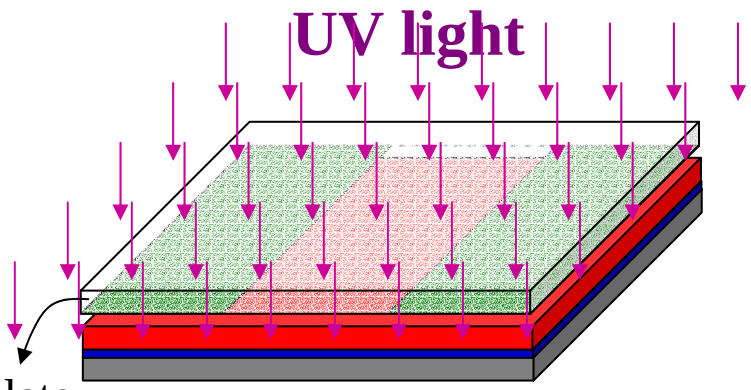


selective dry/wet etching or doping

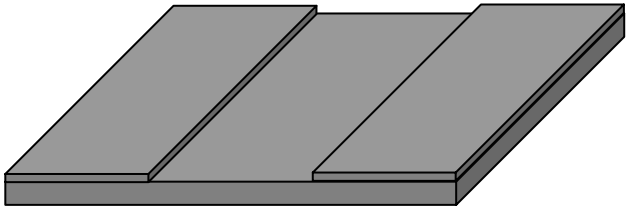
spin-coating



remove resist mask

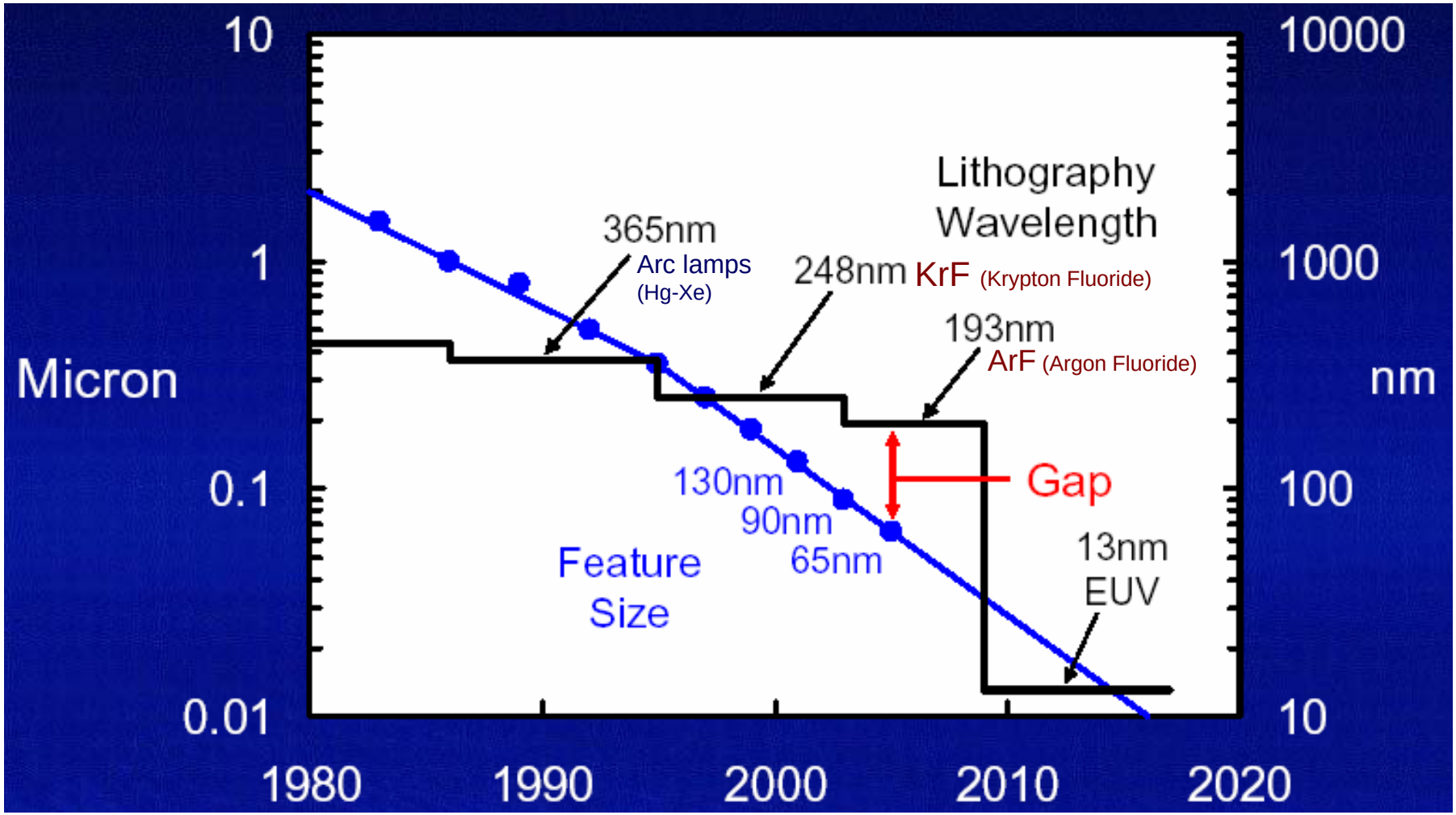


Contact or Projection exposure



finished pattern

SOURCES OF RADIATION
FOR MICROLITHOGRAPHY



Minimum feature size is scaling faster than lithography wavelength

Advanced photo mask techniques help to bridge the gap

Mark Bohr, Intel

The Ultimates of Optical Lithography

Resolution: $R=k_1 (\lambda/NA)$

NA = $\sin\theta$ = numerical aperture

K_1 = a constant for a specific lithography process

smaller K1 can be achieved by

improving the process or resist contrast

Depth of Focus $DoF=k_2 (\lambda/NA^2)$

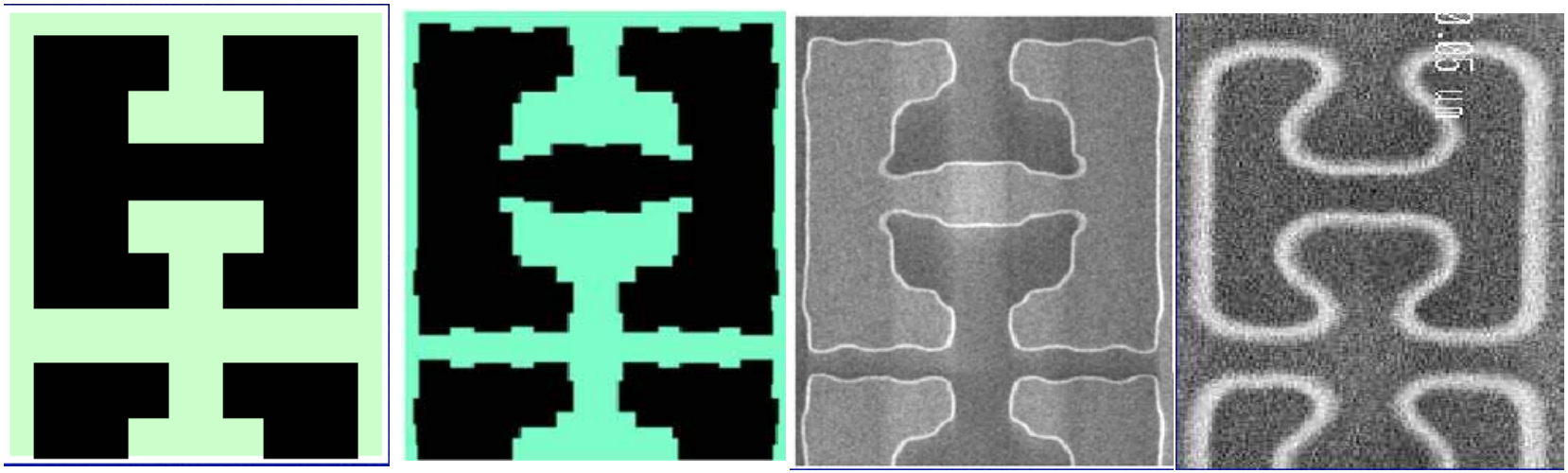
Calculated R and DoF values

UV wavelength	248 nm	193 nm	157 nm	13.4 nm
Typical NA	0.75	0.75	0.75	0.25
Production value of k_1	0.5	0.5	0.5	0.5
Resolution	0.17 μm	0.13 μm	0.11 μm	0.027 μm
DoF (assuming $k_2 = 1$)	0.44 μm	0.34 μm	0.28 μm	0.21 μm

P.F. Carcia et al. DuPoint Photomasks, Vacuum and Thin Film (1999)

Optical Proximity Correction

used in 90 nm (193nm) production line

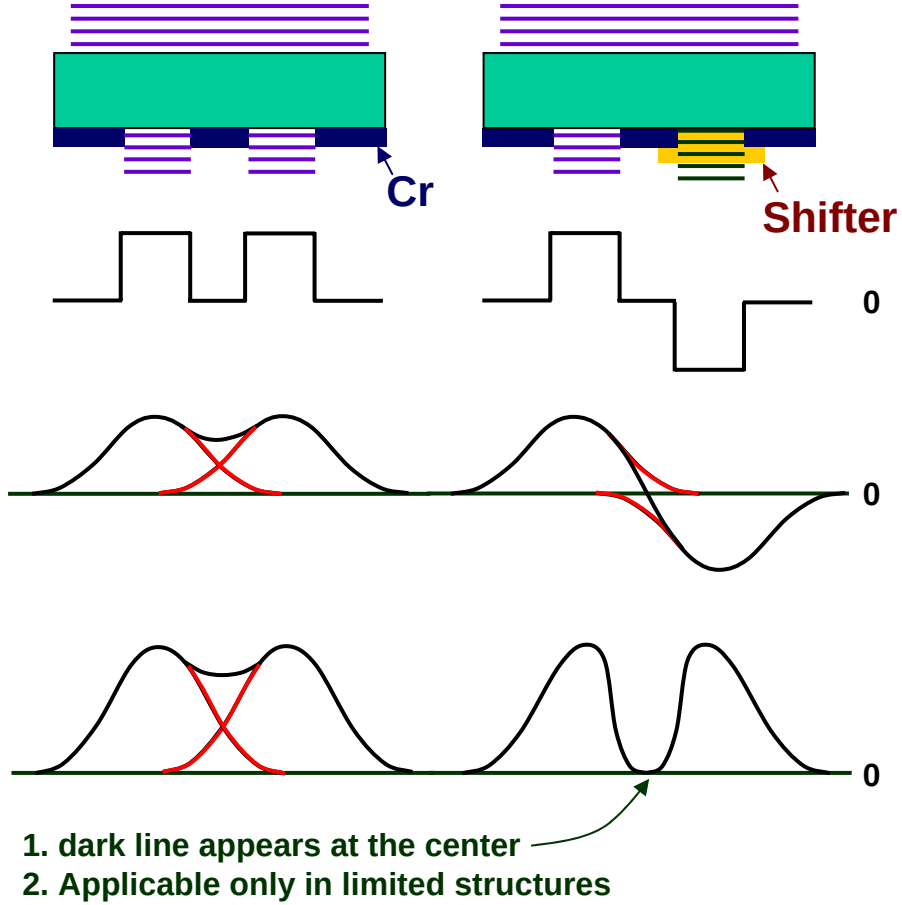


Drawn structure **Add OPC features** **Mask structure** **Printed on wafer**

Mark Bohr, Intel

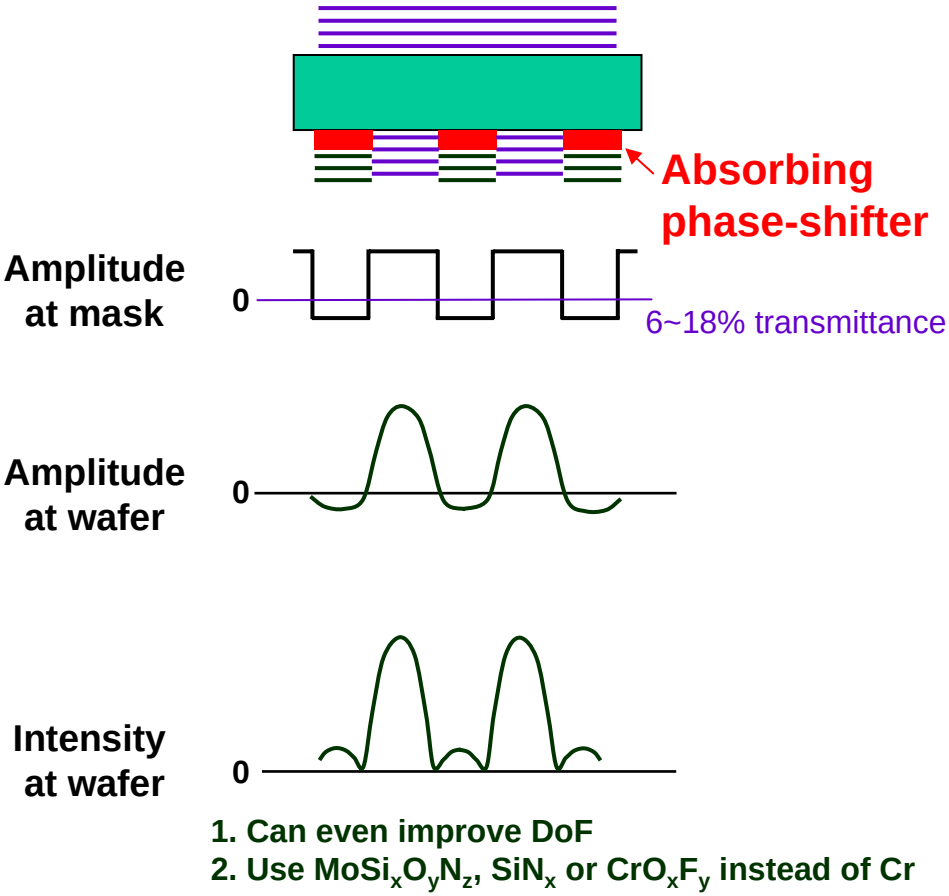
Two types of phase shift mask

Alternating aperture phase shift mask



1. dark line appears at the center
2. Applicable only in limited structures

Embedded attenuating phase shift mask



1. Can even improve DoF
2. Use $MoSi_xO_yN_z$, SiN_x or CrO_xF_y instead of Cr

Ref: P.F. Carcia et al. DuPoint Photomasks, Vacuum and Thin Film

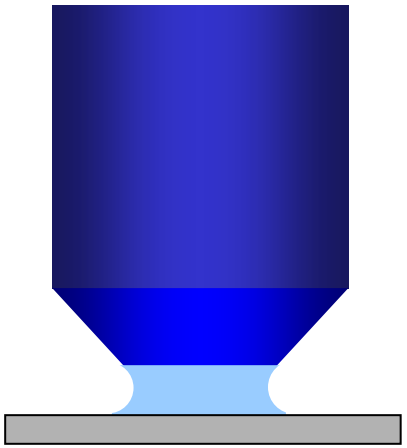
Immersion lithography

Benefits

wavelength is reduced by a factor equal to the refractive index of the medium

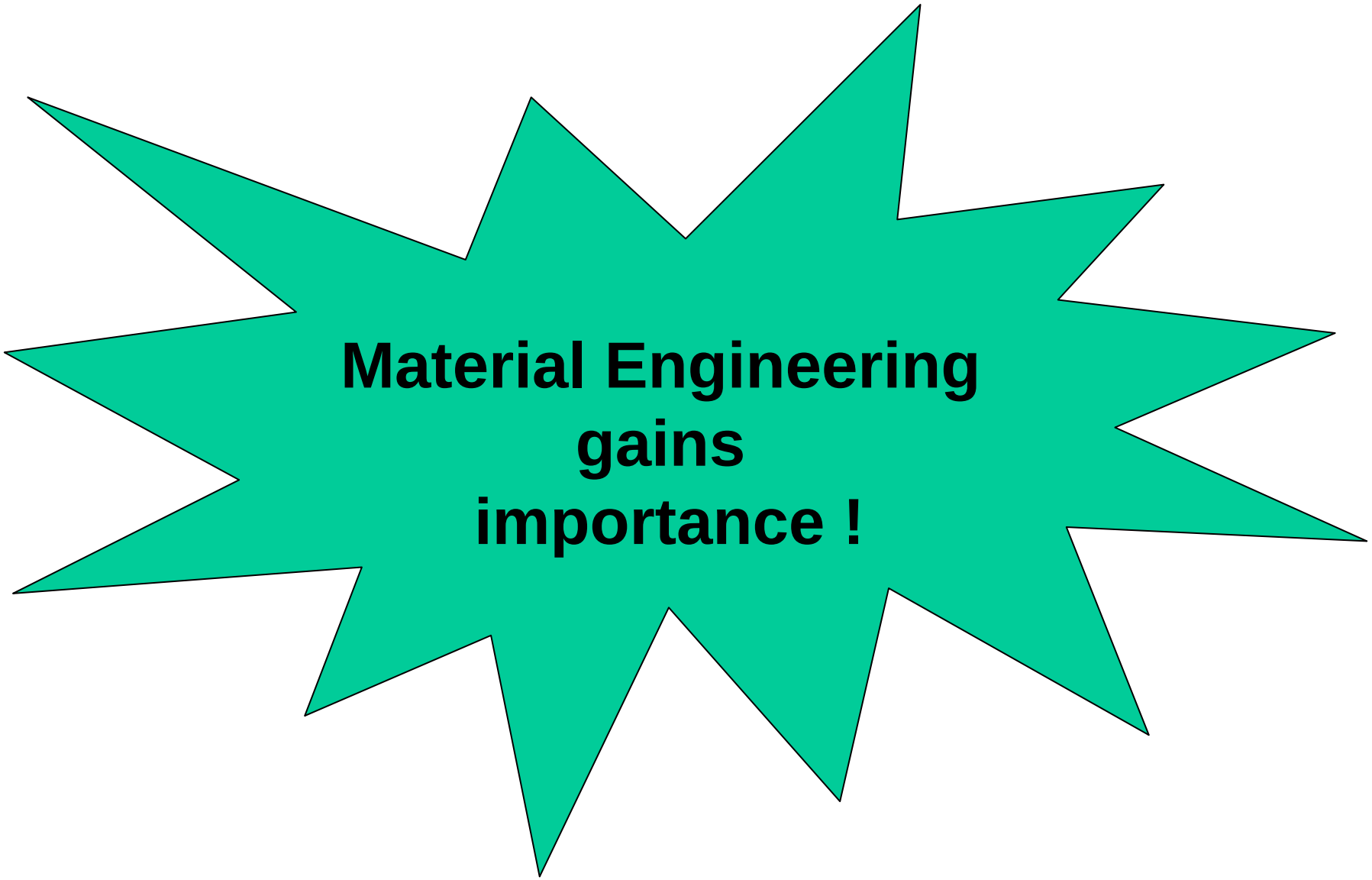
for water $\lambda = \frac{\lambda_{air}}{n_{H_2O}} = \frac{193nm}{1.44} = 134nm$

Depth of focus ~2λ

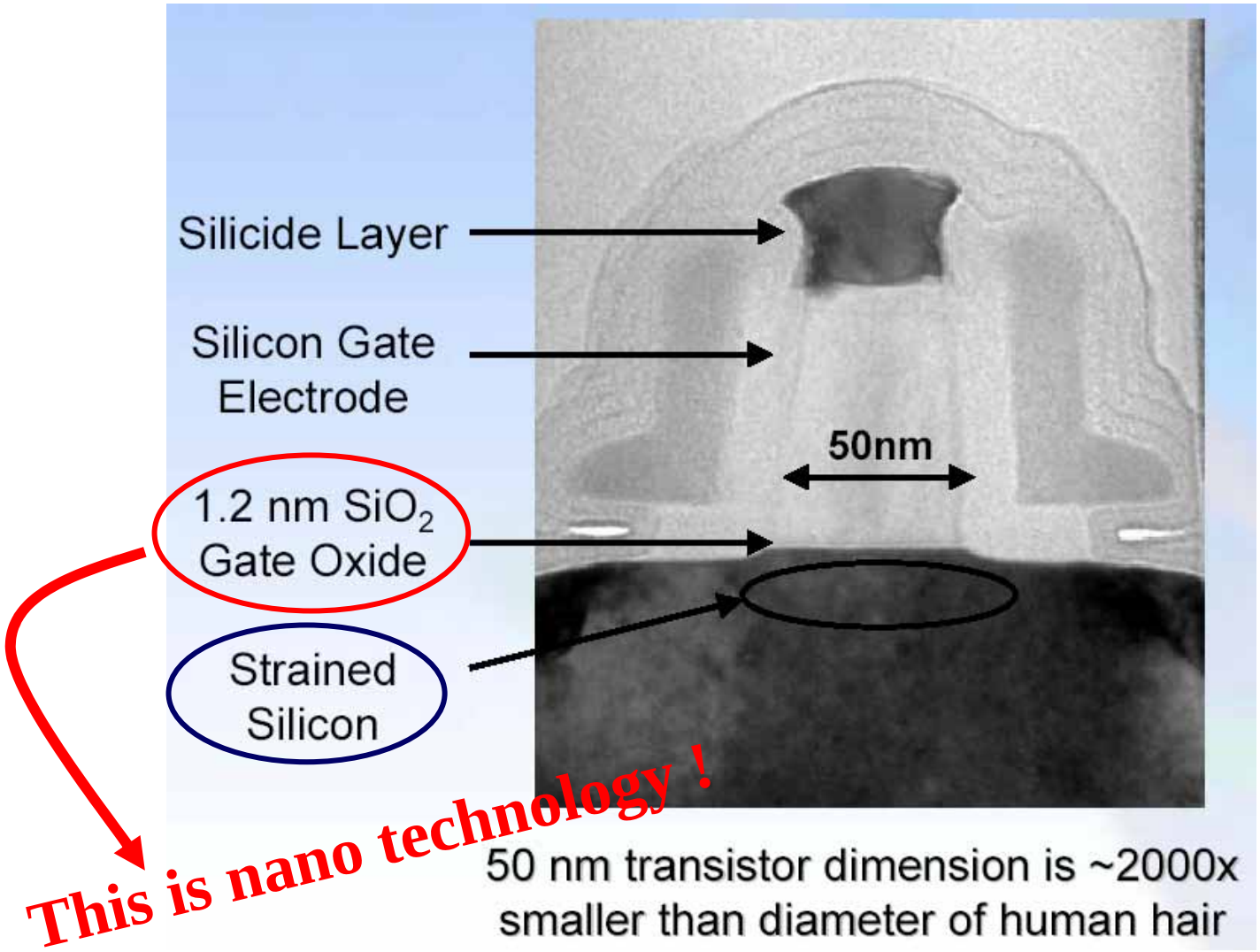


Manufacturing issues

1. **elimination of bubbles in the immersion fluid**
2. **temperature and pressure variations in the immersion fluid**
3. **immersion fluid absorption by the photoresist**
4. **particle generation due to the water dispensing unit**
5. **photoacid generators (PAGs) produced upon exposure extracted into fluid – lens corrosion**
6. **scanning exposure: water left behind (watermarks) and loss of resist-water adhesion (air gap).**


Material Engineering
gains
importance !

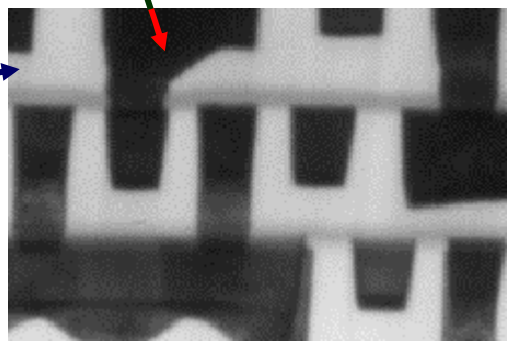
90 nm Generation Transistor



source: Intel develop forum Spring, 2003

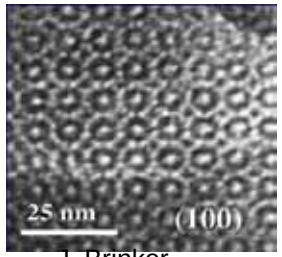
Nano materials will play an important role
in the silicon nanotechnology platform

Interconnectors with high electrical conductivity



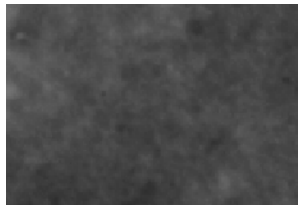
Low K interlevel Dielectric

High K gate oxide

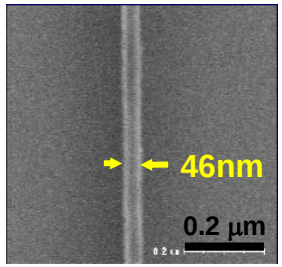


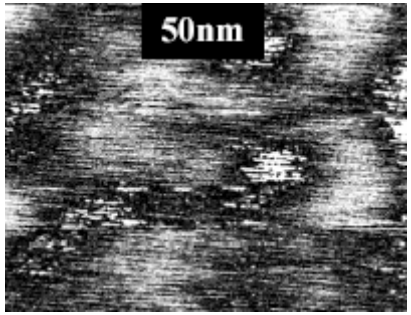
J. Brinker,
UNM/Sandia National Labs

Strained Si



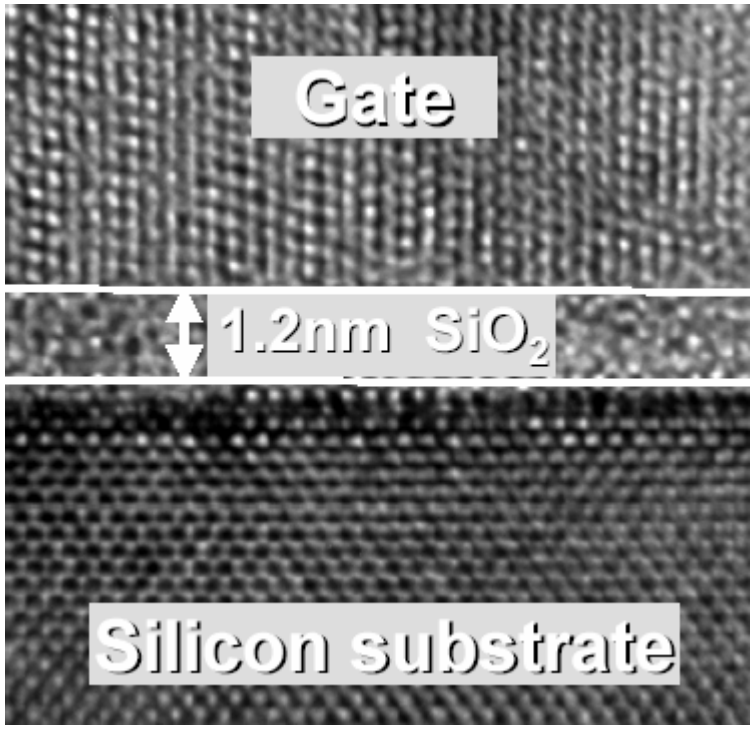
Photoresist

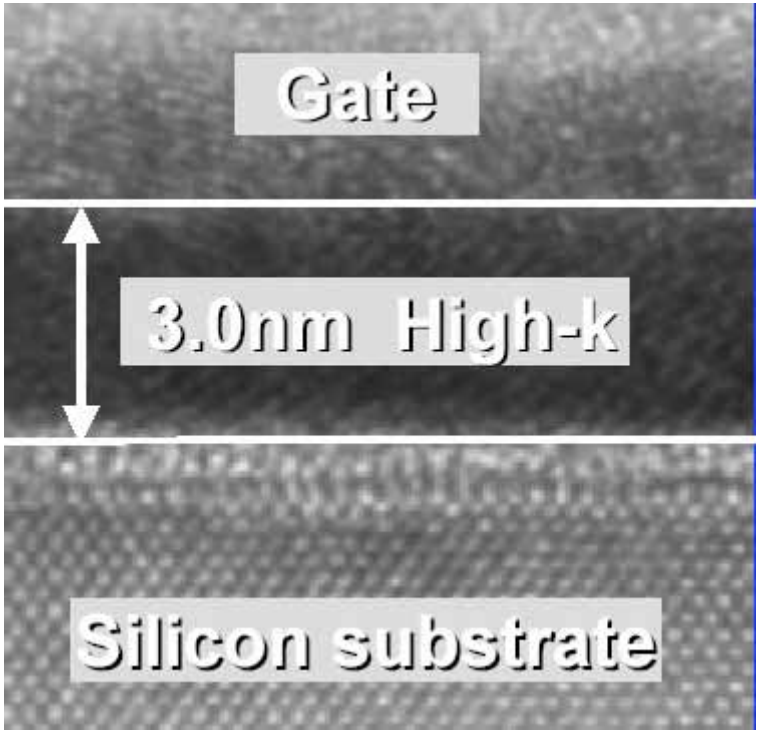




C. Michael Garner, Intel, Sept.16, 2003

Introduction of high-K gate dielectric





	90 nm process	Experimental high-K
Capacitance	1X	1.6X
Leakage	1X	<0.01X

Carolyn Block, Intel

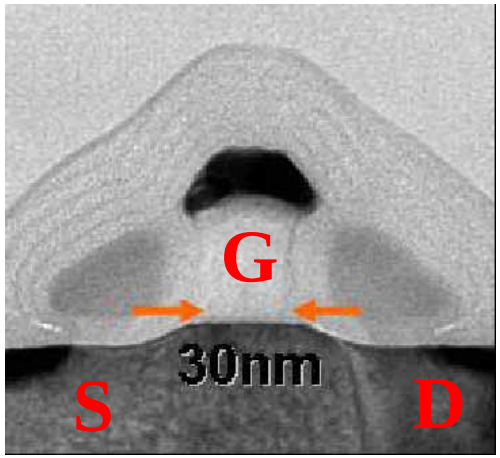
Introduction of new materials

1st Production	1997	1999	2001	2003	2005	2007	2009	2011
Process Generation	0.25 μm	0.18 μm	0.13 μm	90 nm	65 nm	45 nm	32 nm	22 nm
Wafer Size (mm)	200	200	200/ 300	300	300	300	300	300
Inter-connect	Al	Al	Al	Cu	Cu	Cu	Cu	?
Channel	Si	Si	Si	Strained Si	Strained Si	Strained Si	Strained Si	Strained Si
Gate dielectric	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	High-k	High-k	High-k
Gate electrode	PolySi	PolySi	PolySi	PolySi	PolySi	Metal	Metal	Metal

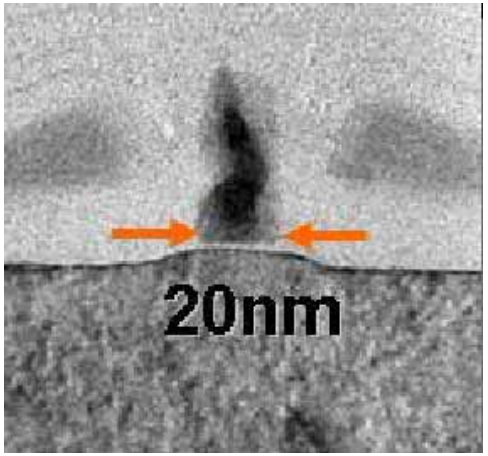
source: Intel develop forum

Experimental transistors for future process generations

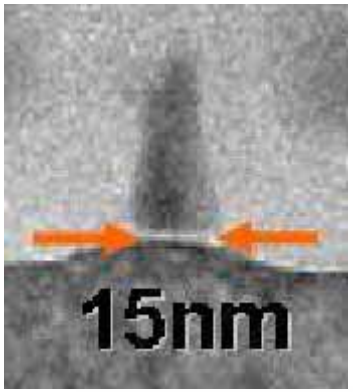
Intel C. Michael Garner Sept. 2003 NanoSIG



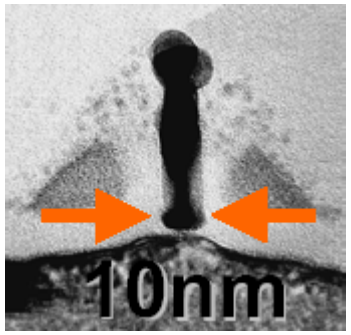
65nm process
2005 production



45nm process
2007 production

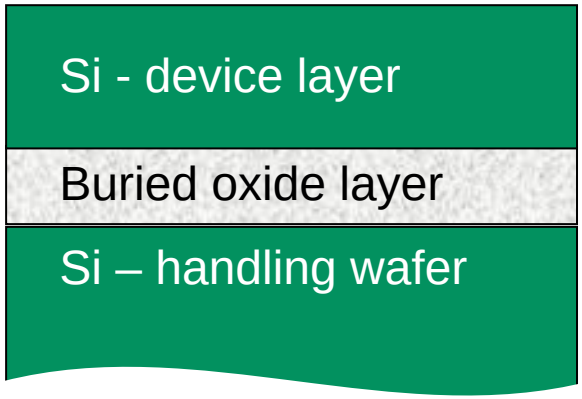


32nm process
2009 production

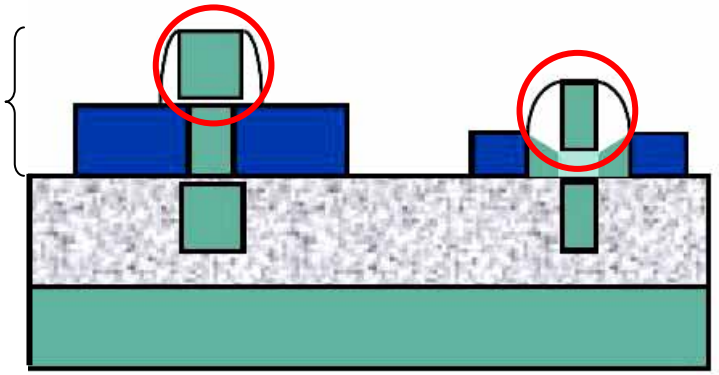


22nm process
2011 production

Silicon-On-Insulator wafer



device layer



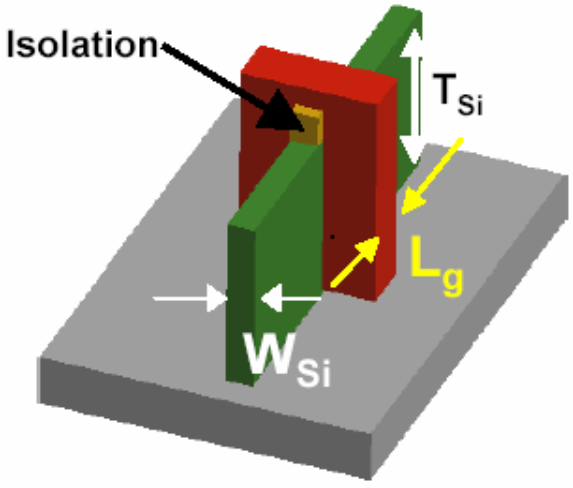
Fully-depleted
ultrathin SOI wafer
L_{gate}=100-50nm
t_{si} = 10-50nm

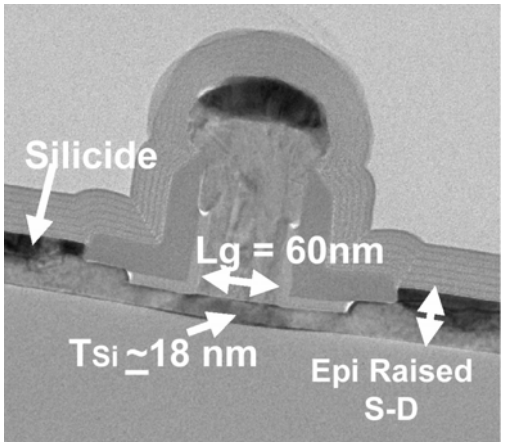
Thin-body
nano SOI wafer
L_{gate}=20-70nm
t_{si} = 5-10nm

M.J. Current et al, Solid state technology, Sep. 2000

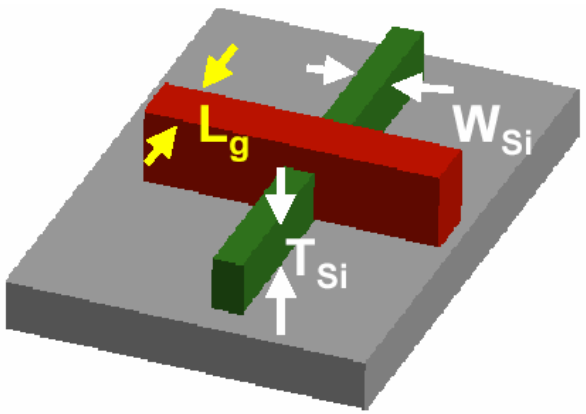
Fully Depleted Transistors made on SOI wafers

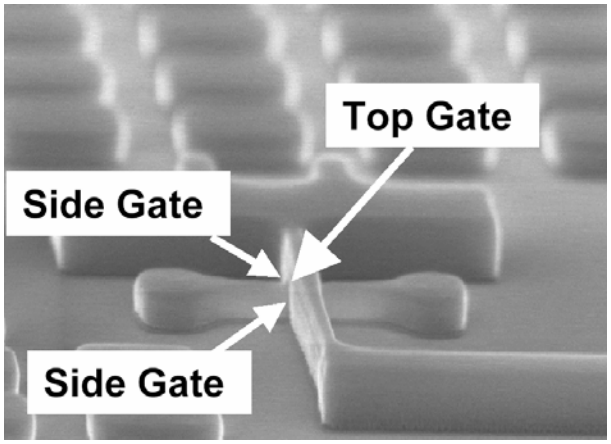
Non-planar Double-gate (FinFET)





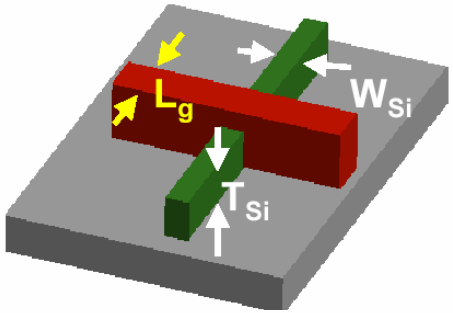
Non-planar Tri-gate



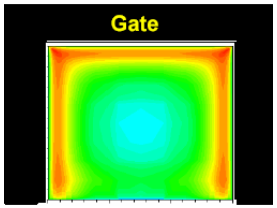


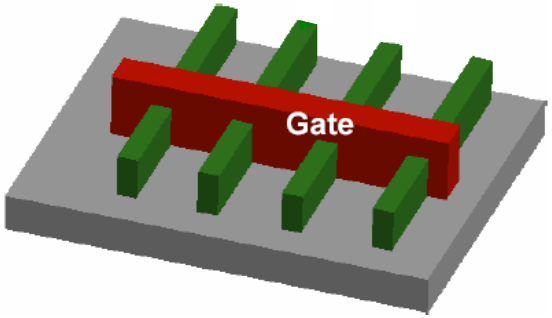
From Tri-gate transistor to Nanowire transistor

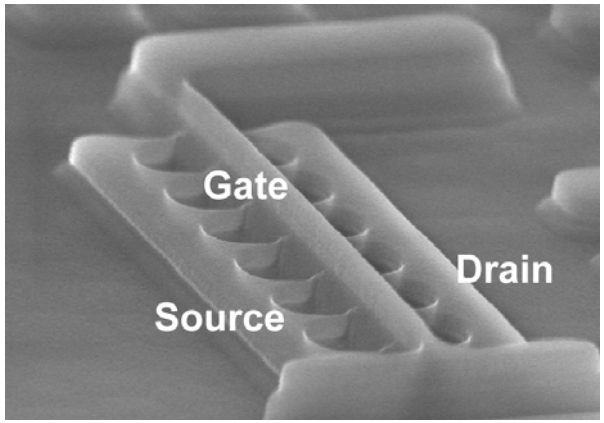
Tri-gate transistor



depletion electric field

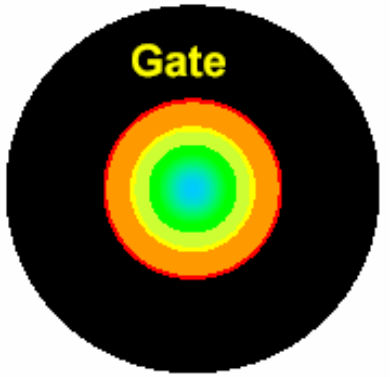


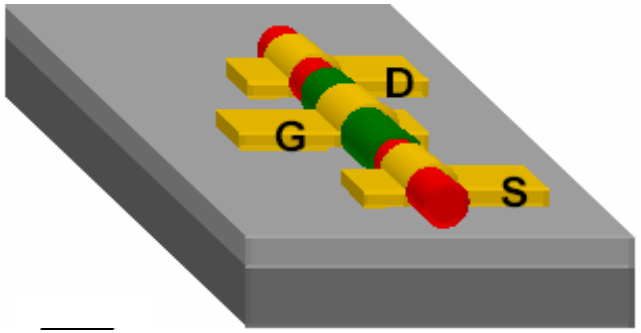




Nano-wire transistor

depletion electric field





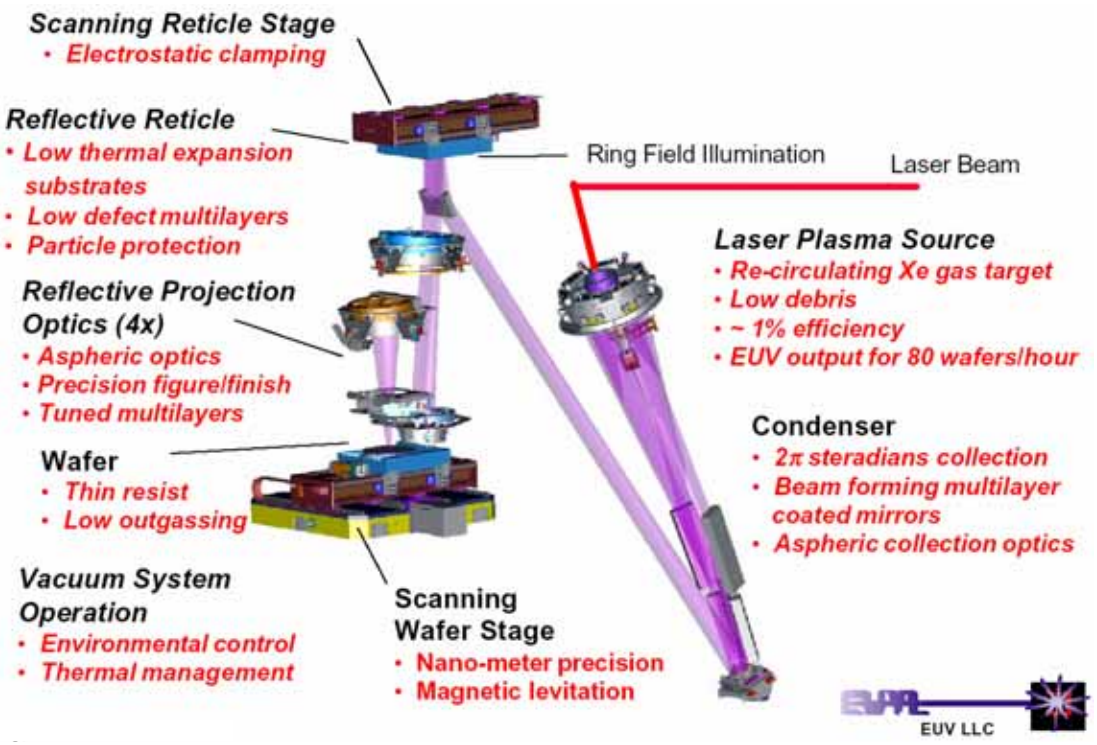
Robert Chau, Intel, 61st Device Research Conference June 2003

Future light sources:

Extreme UV

Electron beam

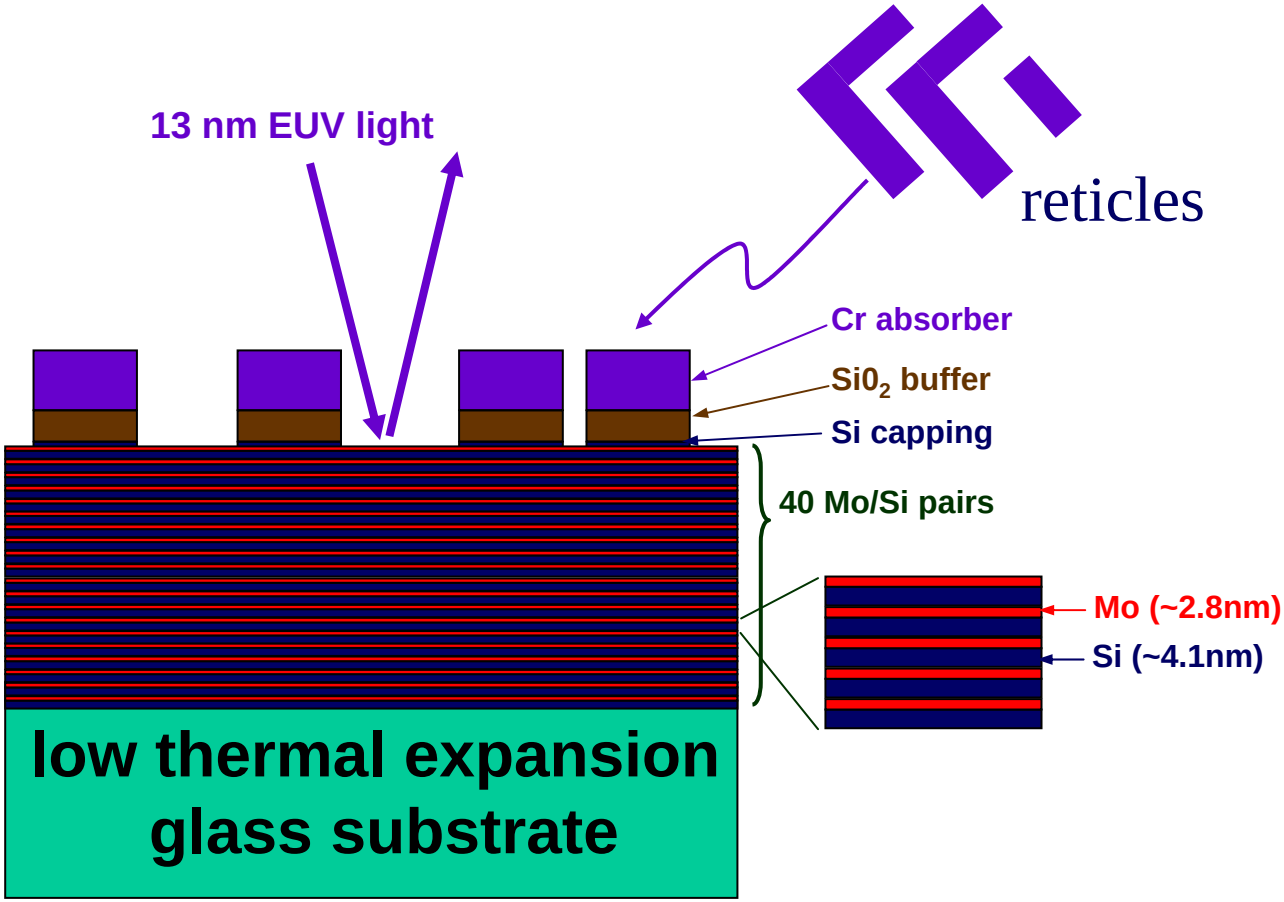
EUV exposure tool



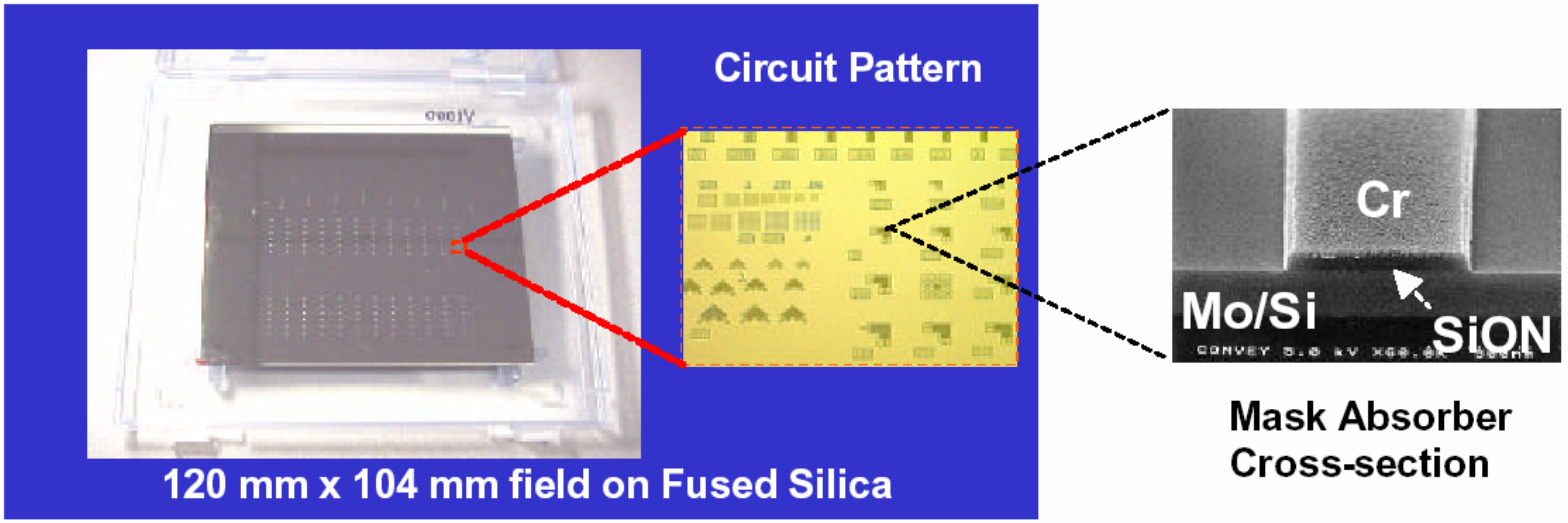
- **Uses very short 13.4 nm light**
- **13.4 nm radiation absorbed by all materials**
- **Requires reflective optics coated with quarter-wave Bragg reflectors**
- **Uses reflective reticles with patterned absorbers**
- **Vacuum operation**

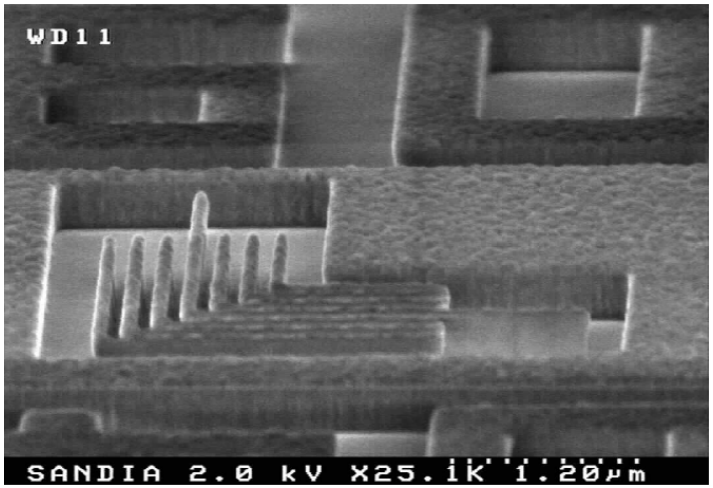
EUV reflective mask

Intel EUV mask

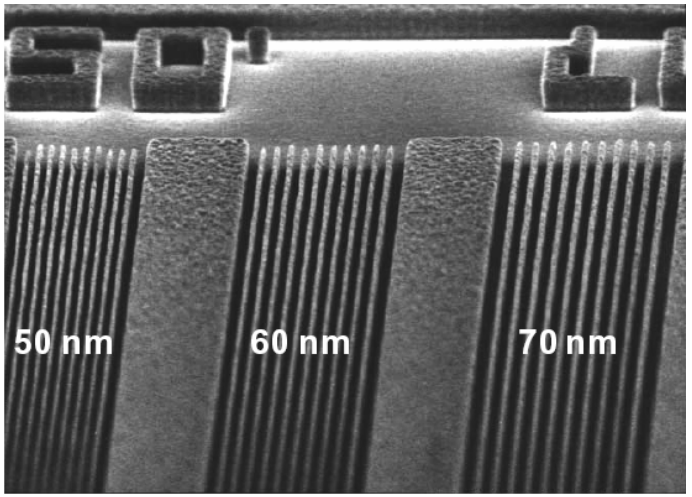


EUV mask and patterned resist





90 nm Elbows in 350 nm polySi



Source: **Intel**

Electron-Beam Lithography

Electron Beam (e-beam) Gun:

Electrons generated by:

- Thermionic emission from a hot filament.
- Field aided emission by applying a large electric field to a filament.
- Or a combination of the two.

Filament is negatively biased (cathode) and electrons are accelerated to the substrate at typically 25 - 100 keV.

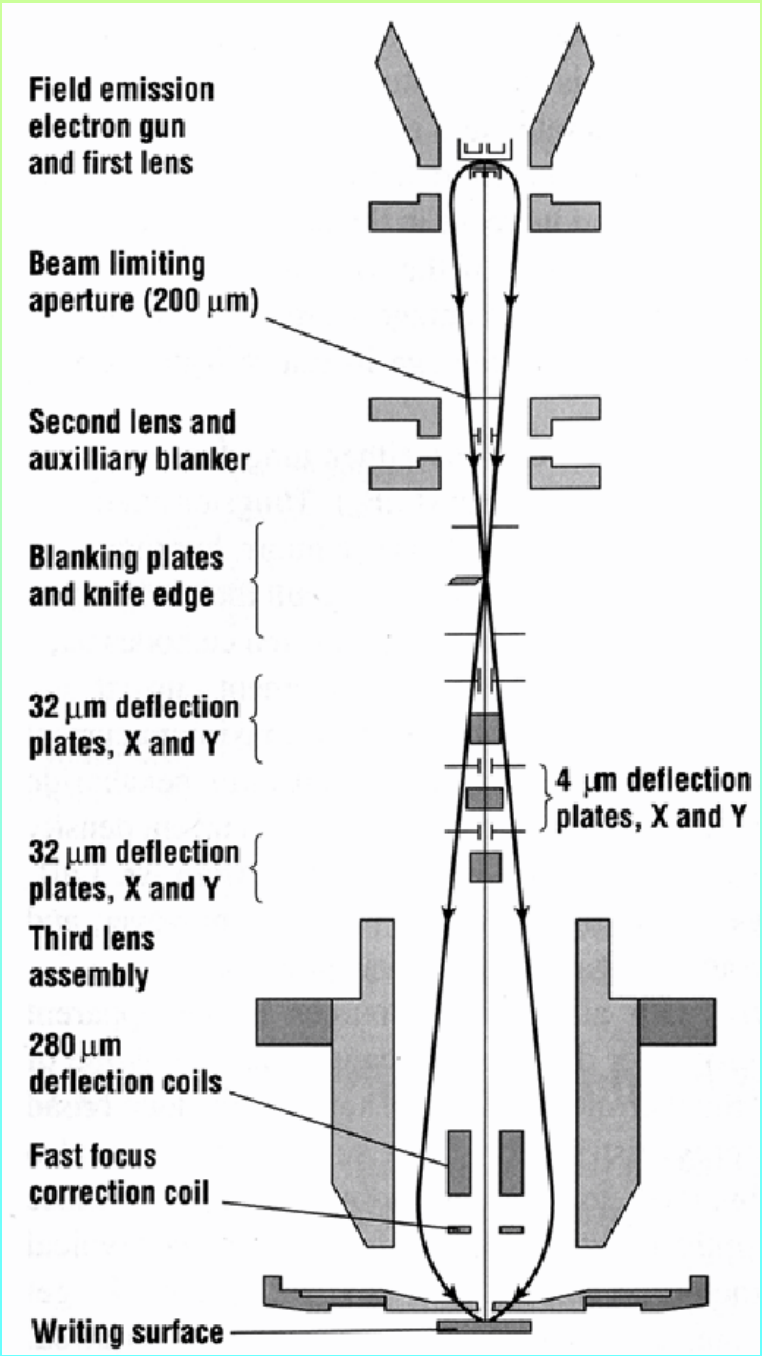
$$eV = \hbar^2 k^2 / 2m_e \Rightarrow \lambda \approx 0.25 \sim 0.12\text{nm}$$

E-beam is focused to a small spot size using:

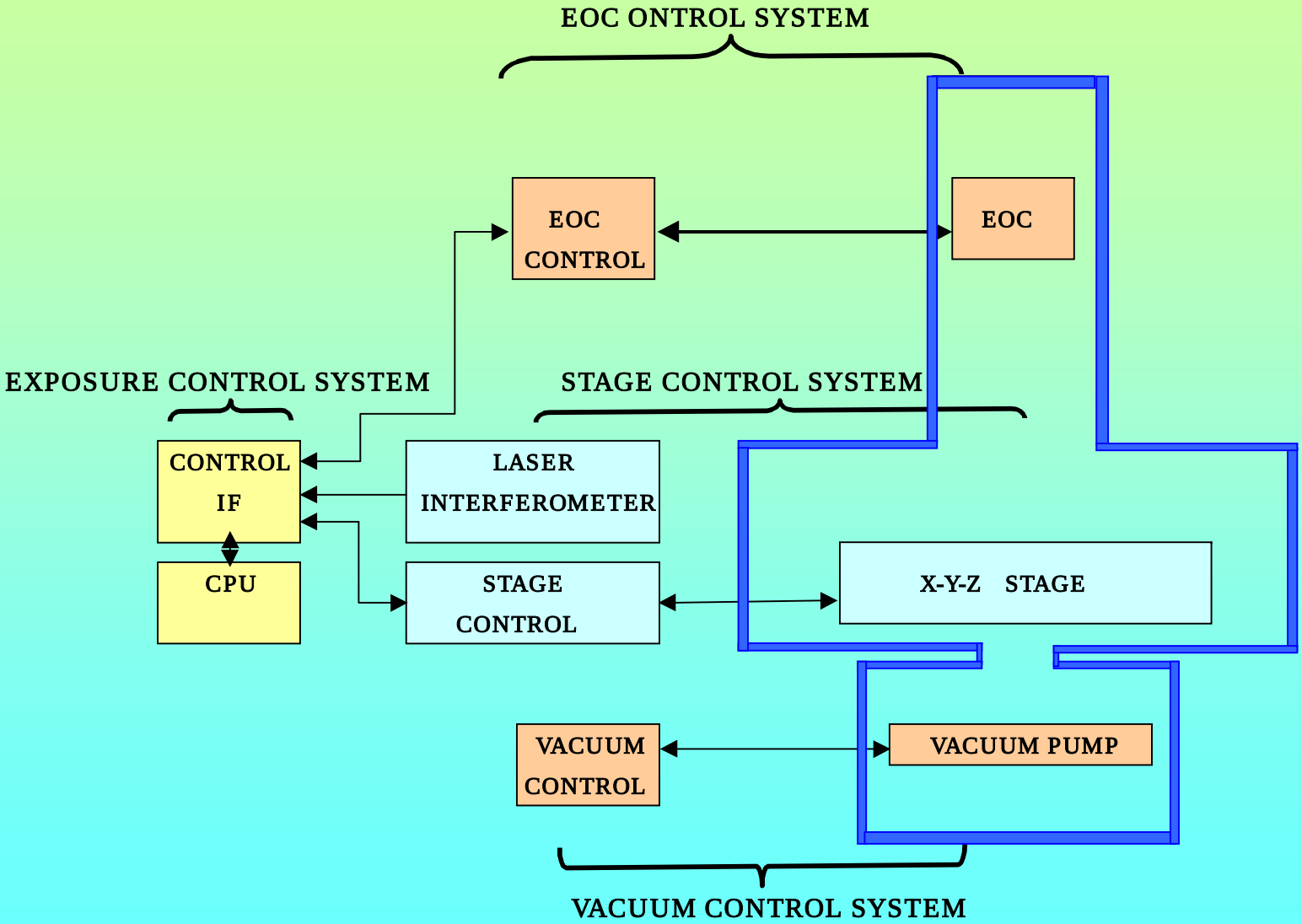
- Electrostatic lenses
- Magnetic fields
- Apertures

A scanned e-beam spot "writes" the image in the resist one "pixel" at a time.

X,Y direction of beam is controlled by electrostatic plates.



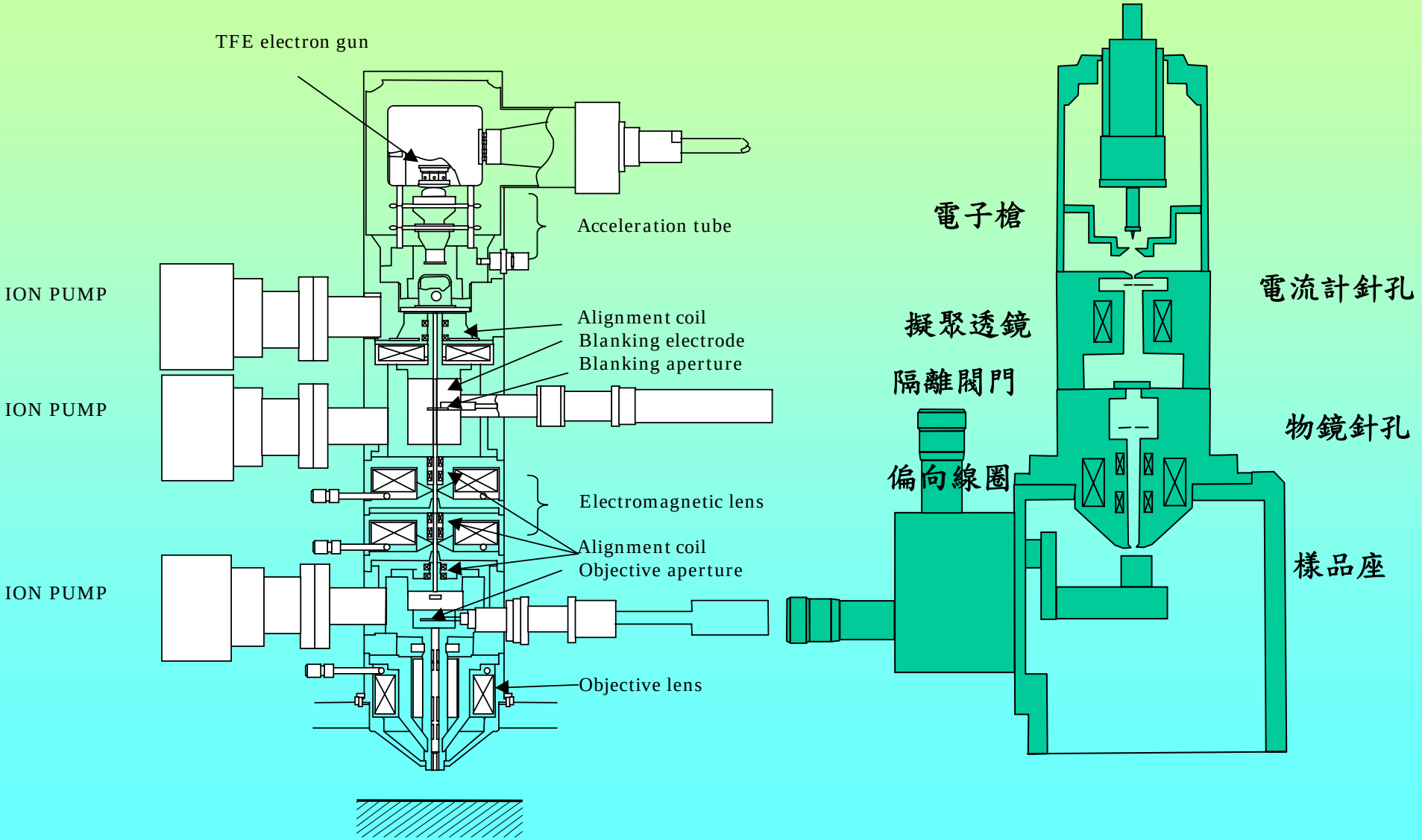
ELECTRON BEAM LITHOGRAPHY SYSTEM



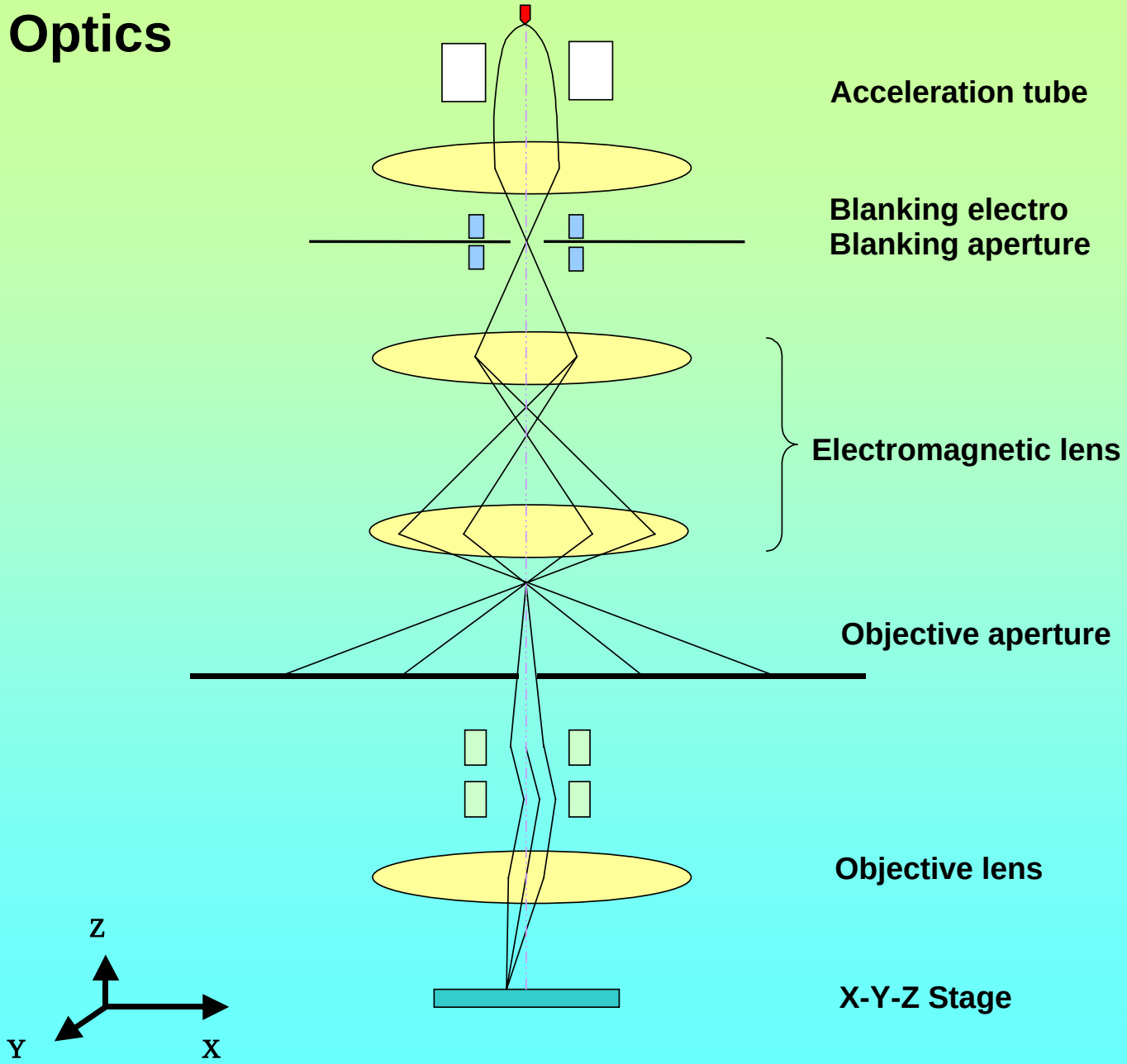
JEOL JBX-9300FS

ELIONIX ELS-7000

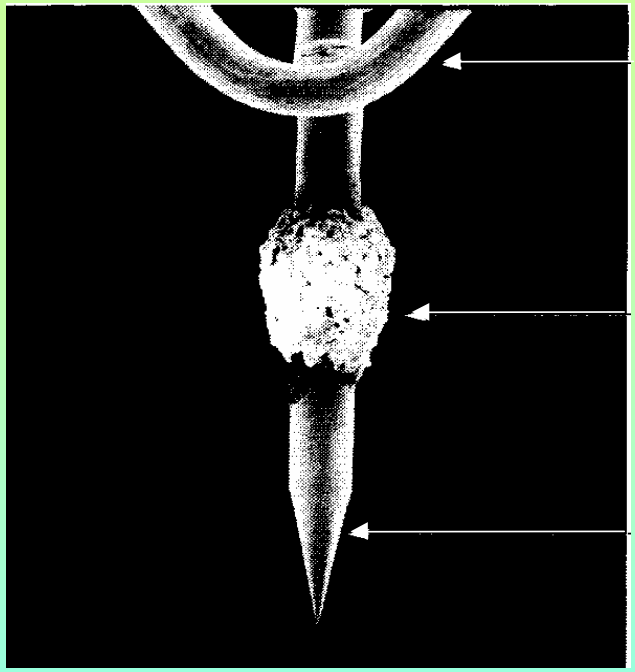
ELECTRON OPTICS SYSTEM



Electron Optics



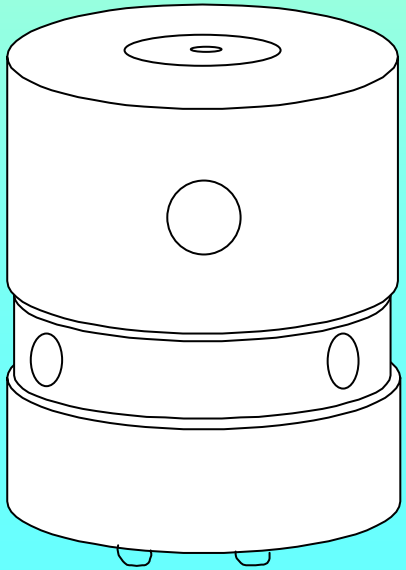
ZrO/W THERMAL FIELD EMISSION GUN

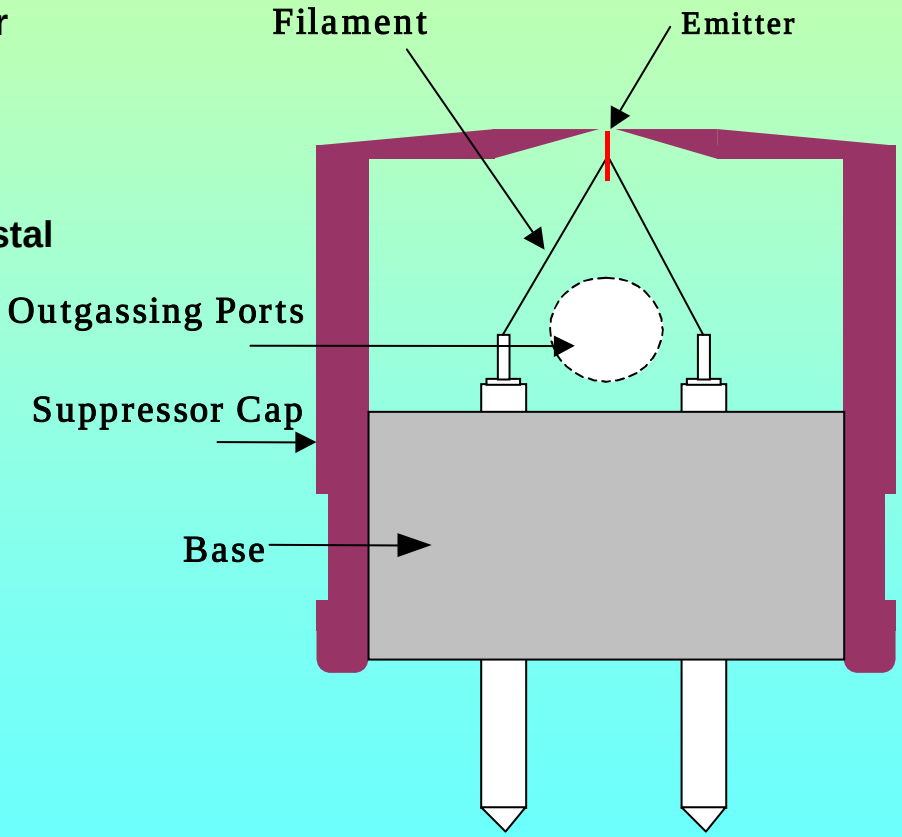


Polycrystalline tungsten
Heating filament

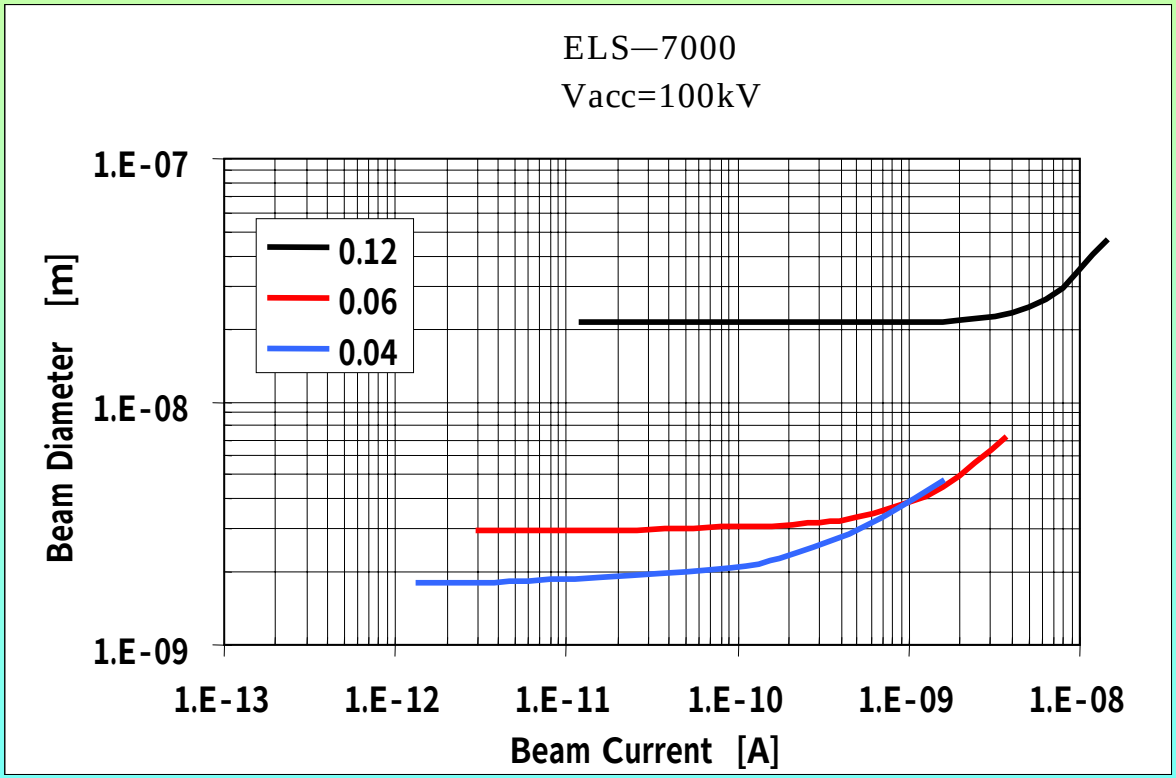
ZrO Reservoir

<100> W Crystal

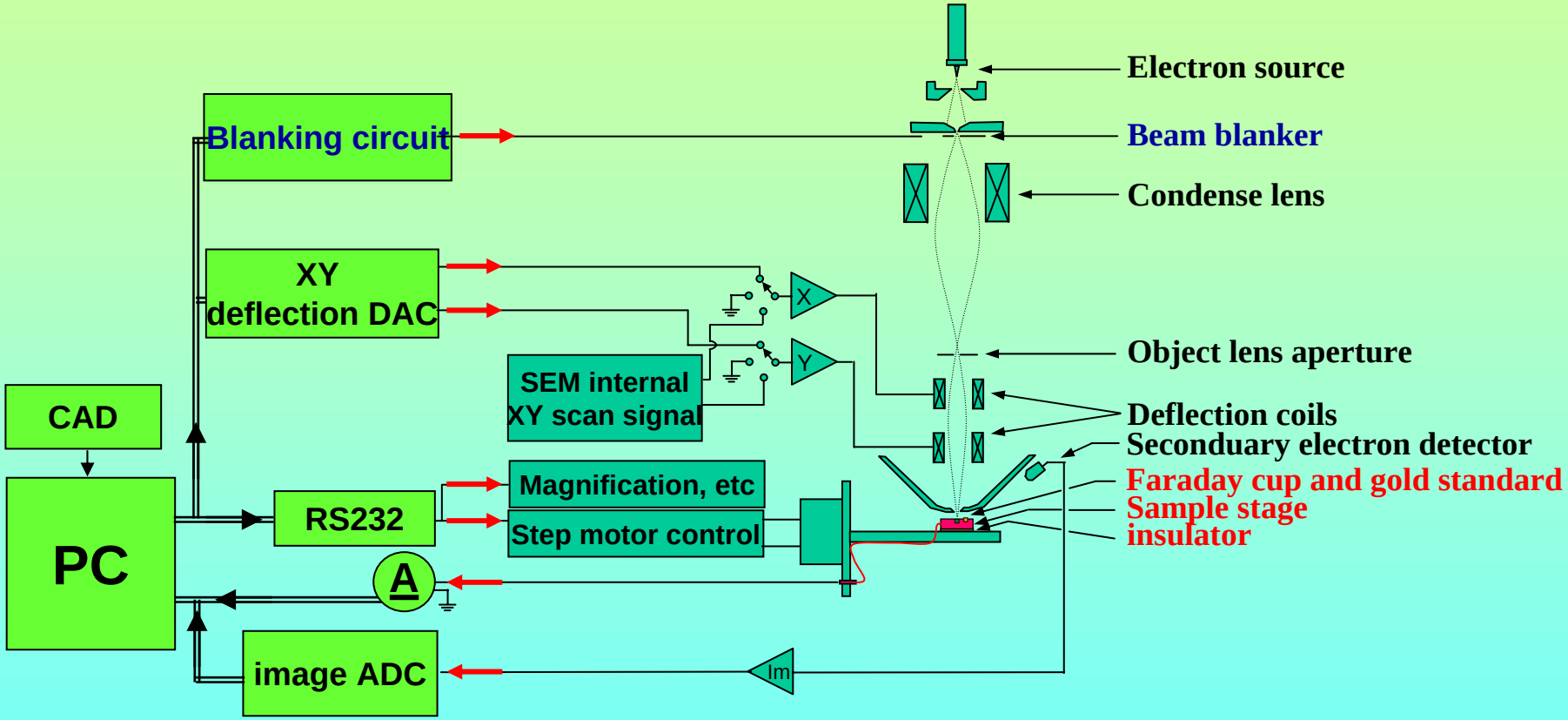




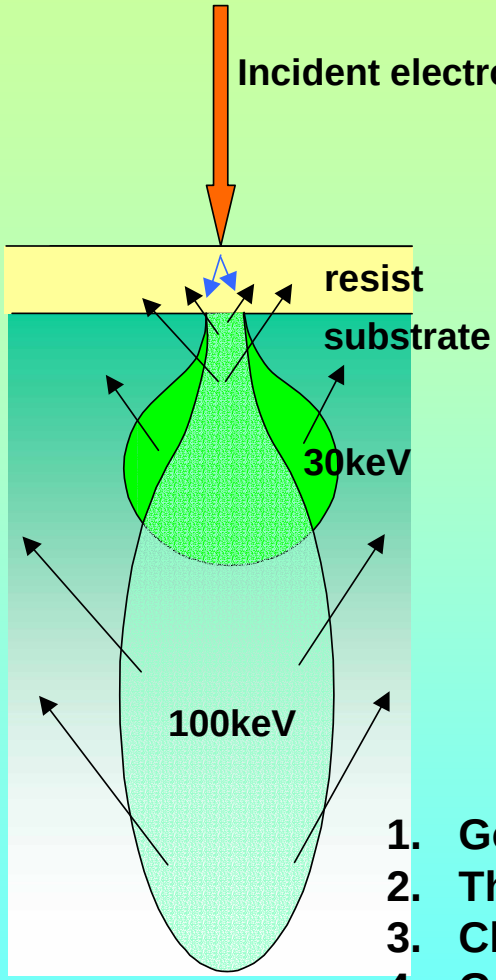
Beam spot size vs. beam current for different apertures

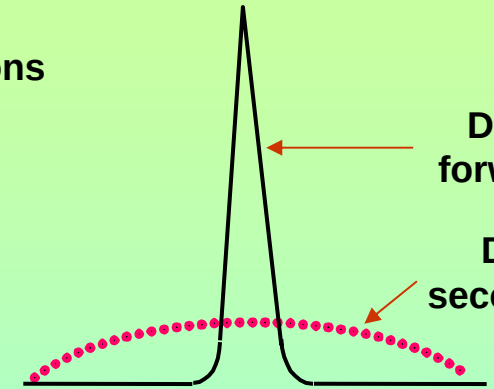


Modification of an SEM based e-beam writer



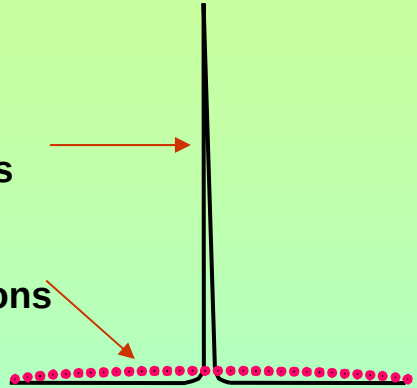
Comparison between 30keV and 100keV e-beam writer





30keV

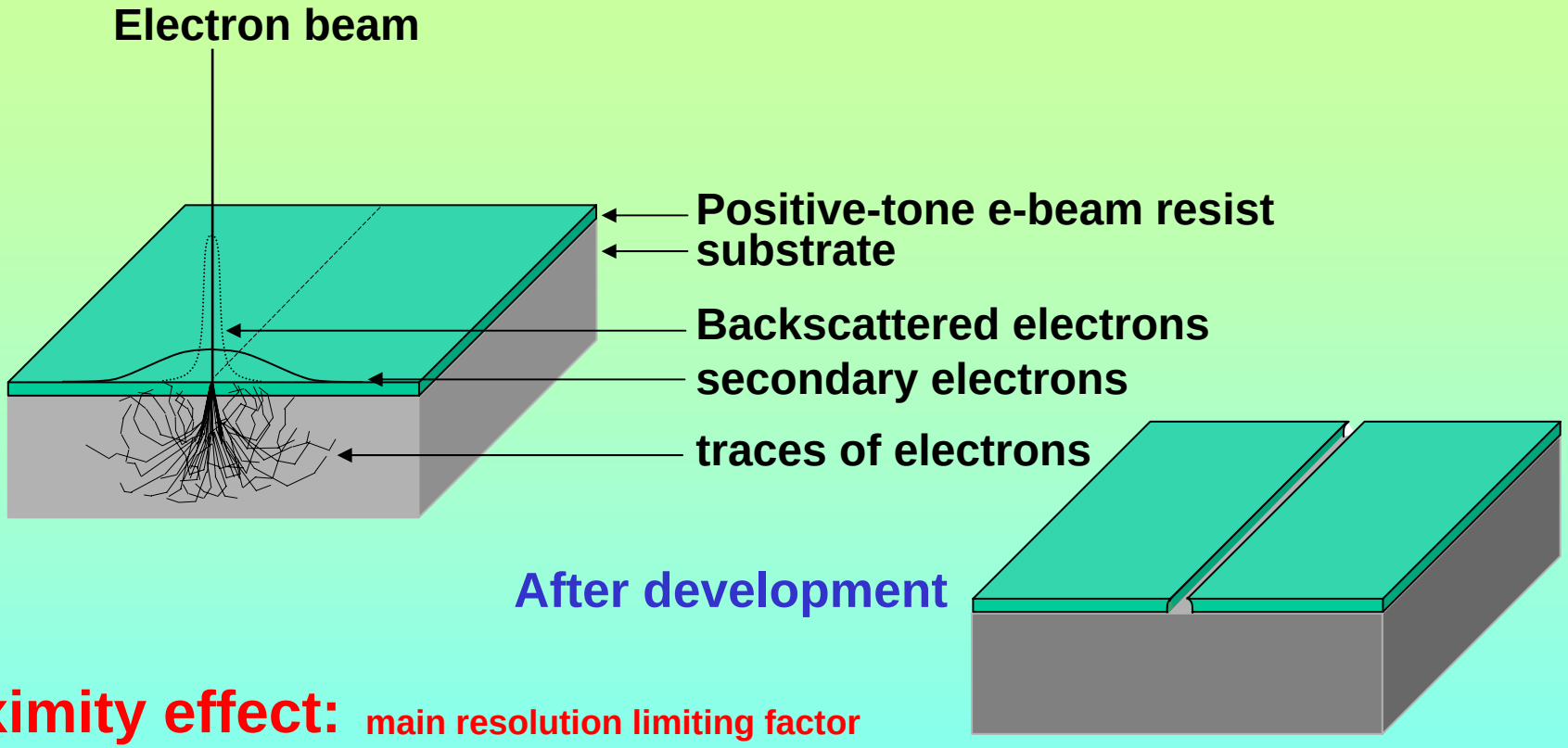
1. Good for prototype test
2. Thin resist line-width < 30nm
3. Clear align key image
4. Good for lift-off process
5. Lack of stage stability



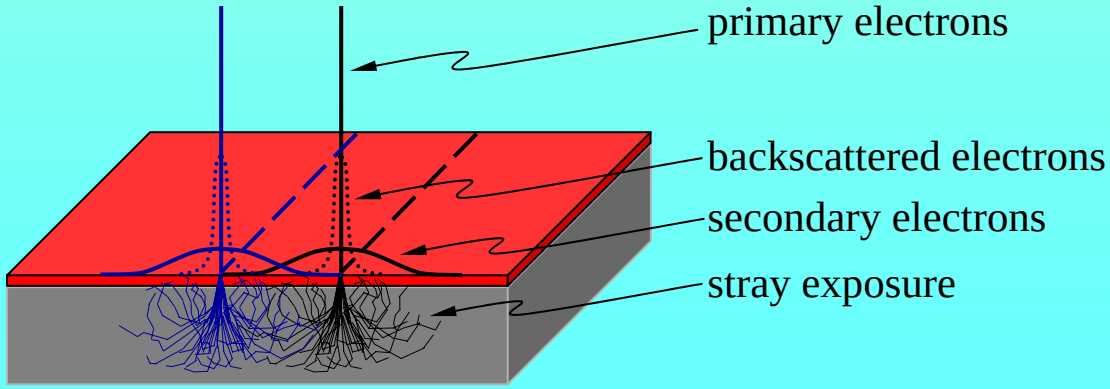
100keV

1. Good for large area exposure
2. Thin resist line-width < 10nm
3. Require thick/clear align keys
4. Require extra resist engineering
5. Stable/accurate stage stability

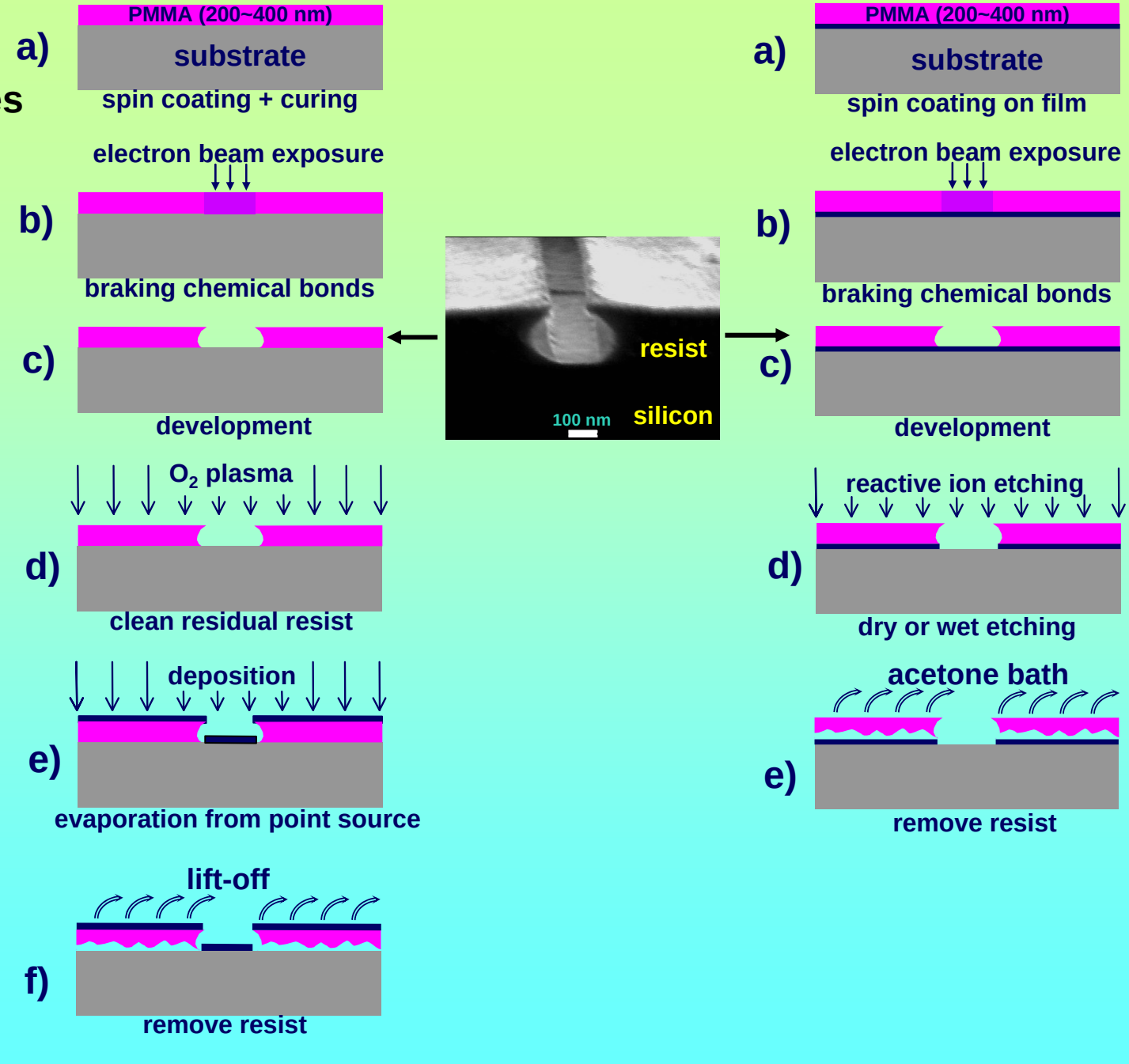
Principal of Electron Beam Exposure



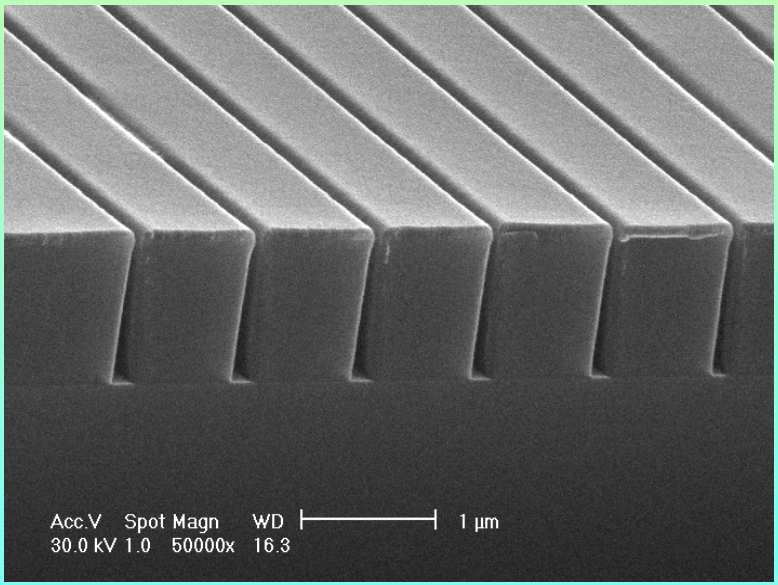
Proximity effect: main resolution limiting factor

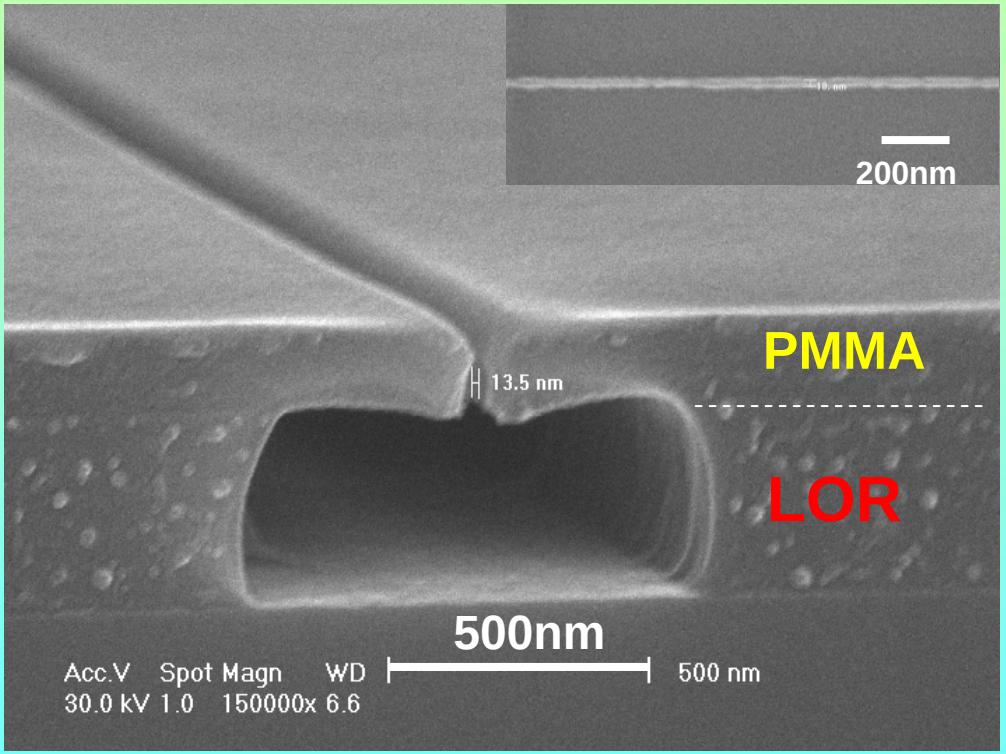


Lift-off and Etching processes

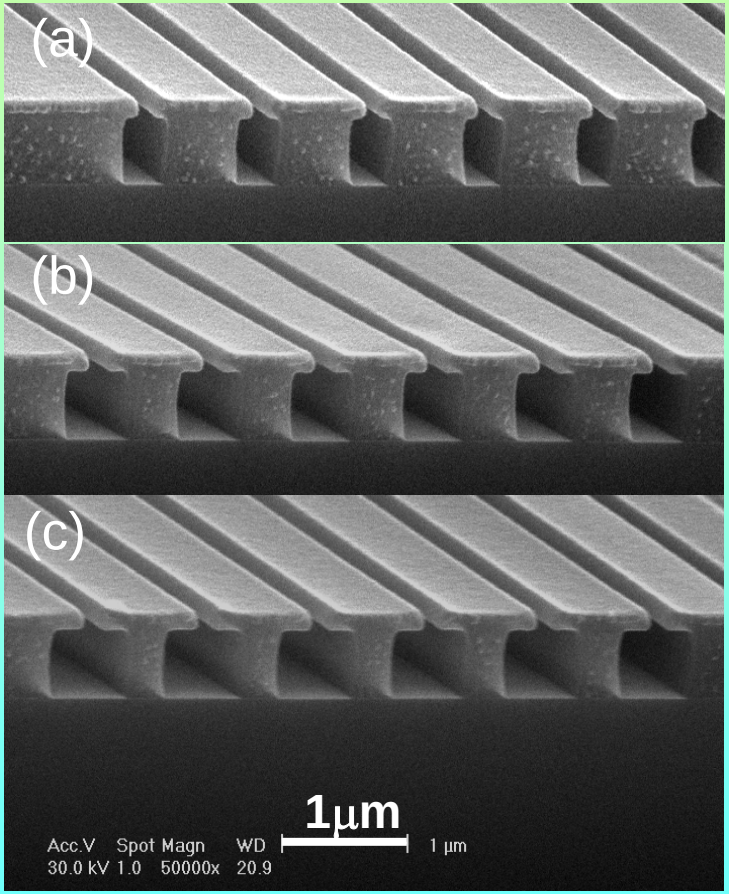


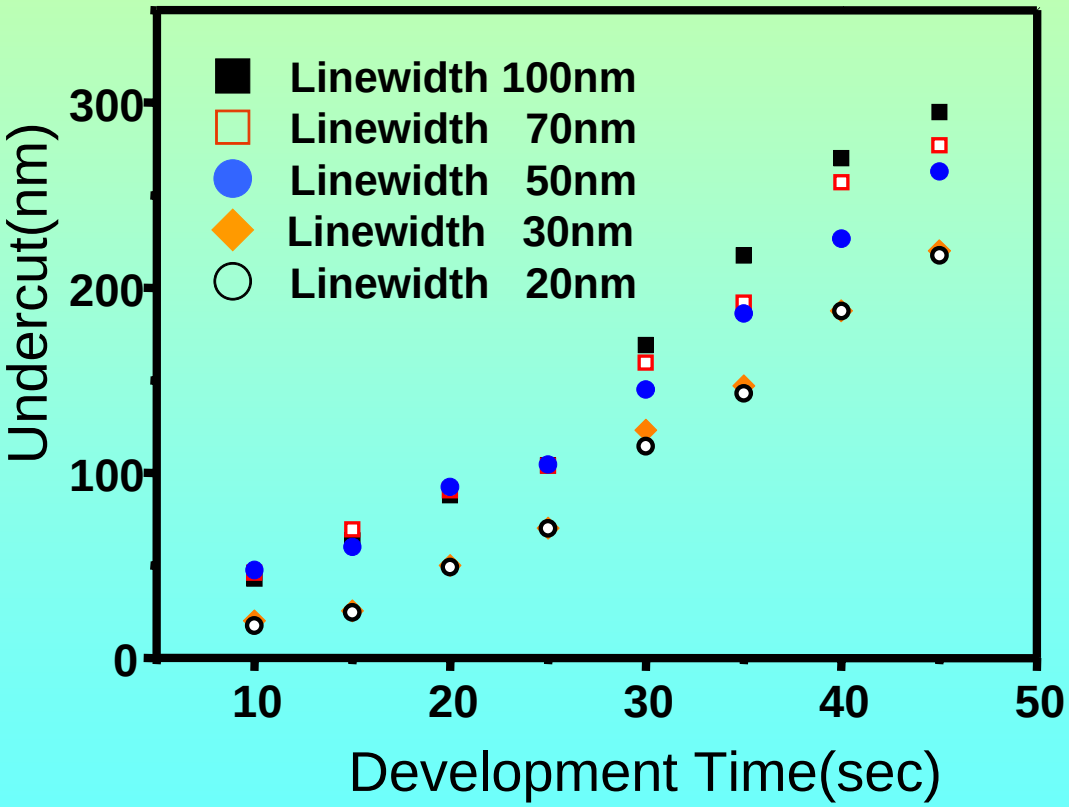
Resist profile made by high energy beam exposure



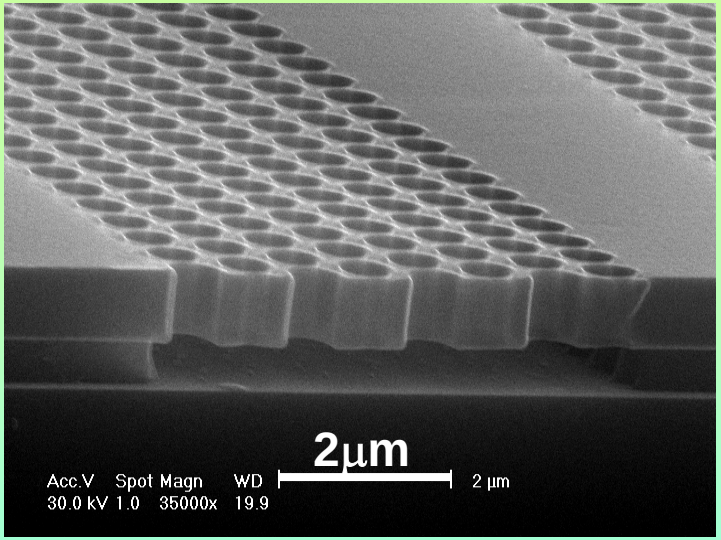


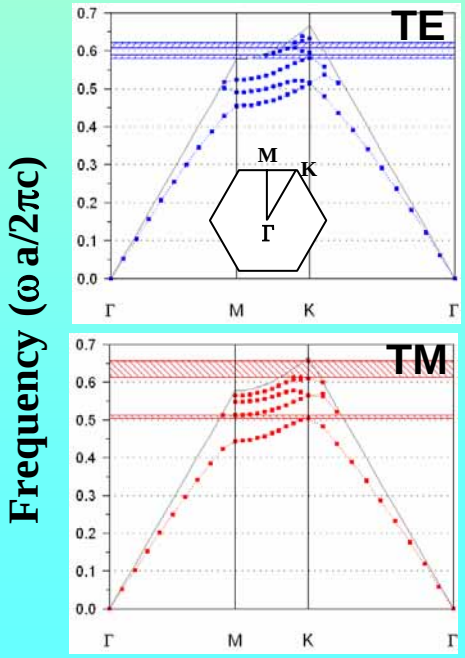
Controlling undercut in bottom layer resist



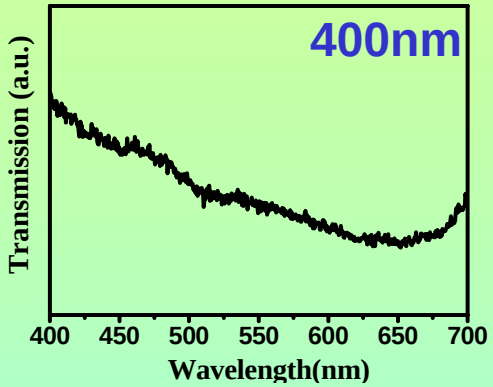


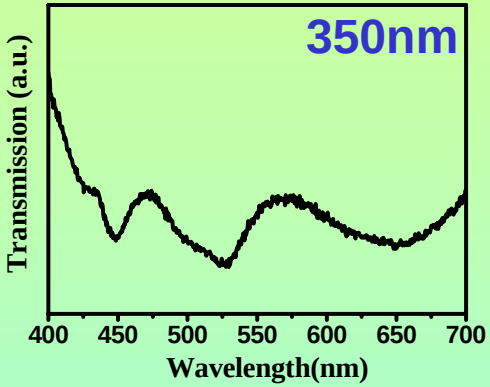
quasi-3D polymer photonic crystal

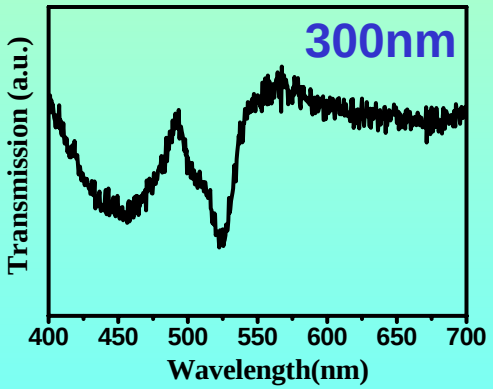


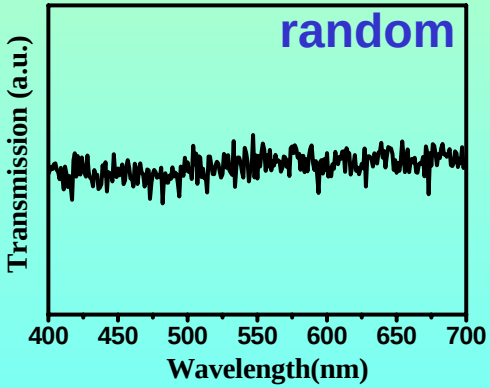


Transmission spectra, different lattice constants

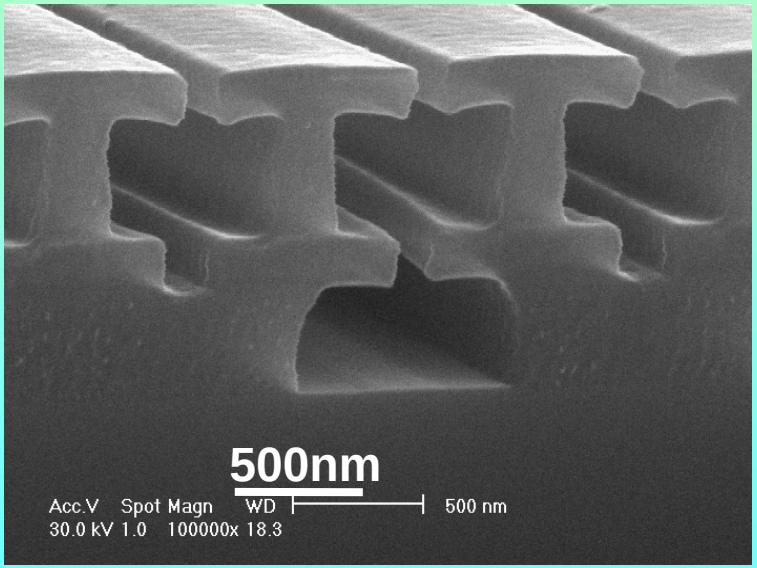




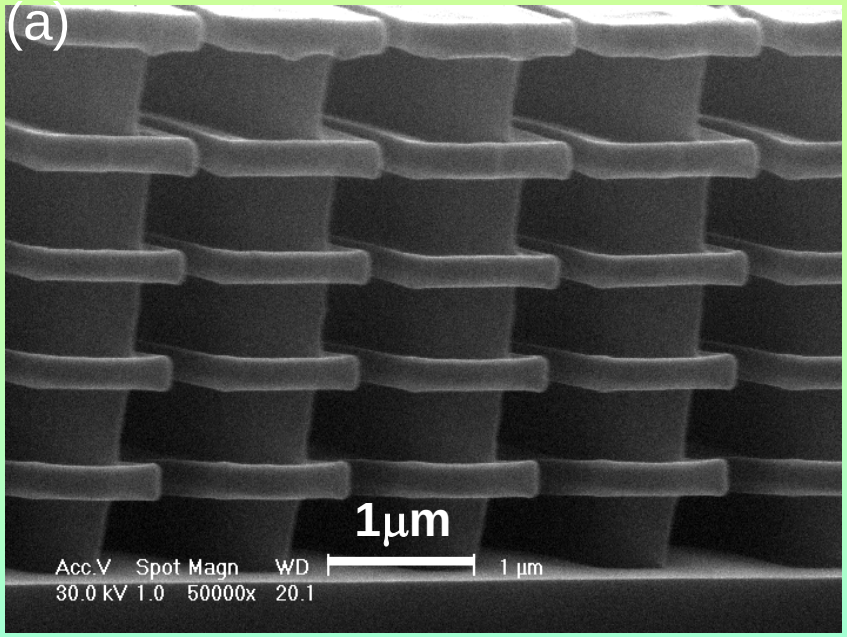


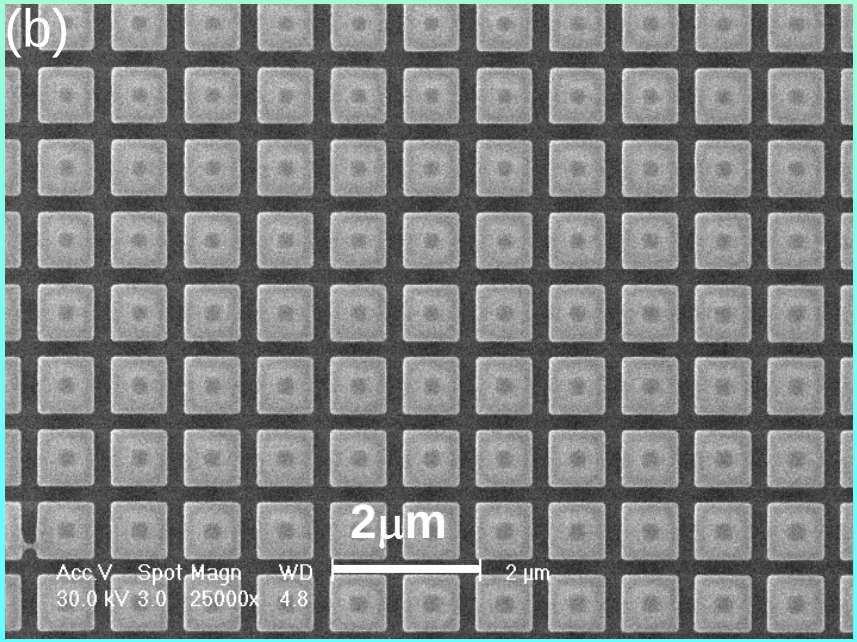


3D polymer structures



Advanced Materials 19, 3052–3056 (2007)





Examples of 100keV e-beam lithography

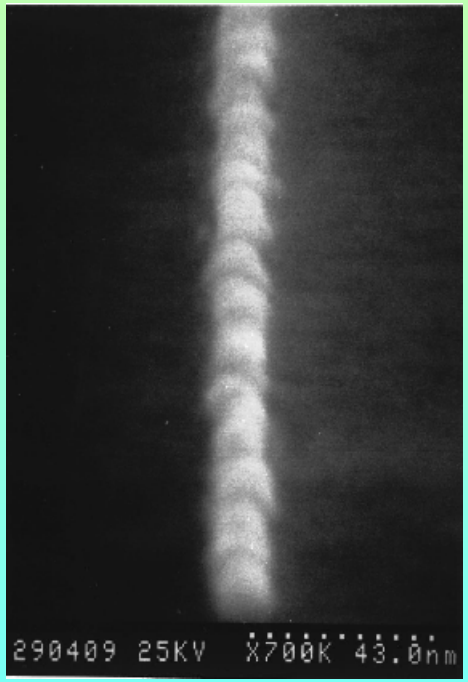
3nm NiCr wire

D. R. S. Cumming et al,
Microelectronic Engineering 30 (1996), 423

Machine : Modified JEOL 100CXII

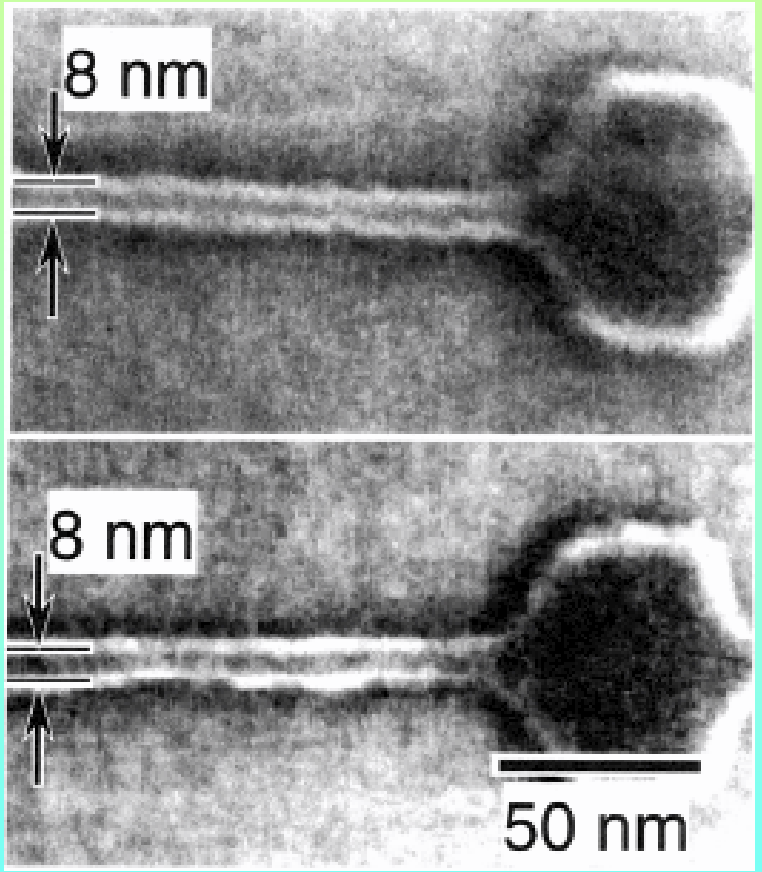
Kelvin Nanotechnology Ltd

13nm Au wire



M. Kamp et al.
J. Vac. Sci. Technol. B, 17, 86, (1999)
Machine : Eiko E 100

8 nm negative-tone inorganic resist



M. S. M. Saifullah et al., Jpn. J. Appl. Phys. **38** (1999) 7052.
K. Yamazaki et al., Proc. SPIE. **3997** (2000) 458.

Machine : 100-keV e-beam writer

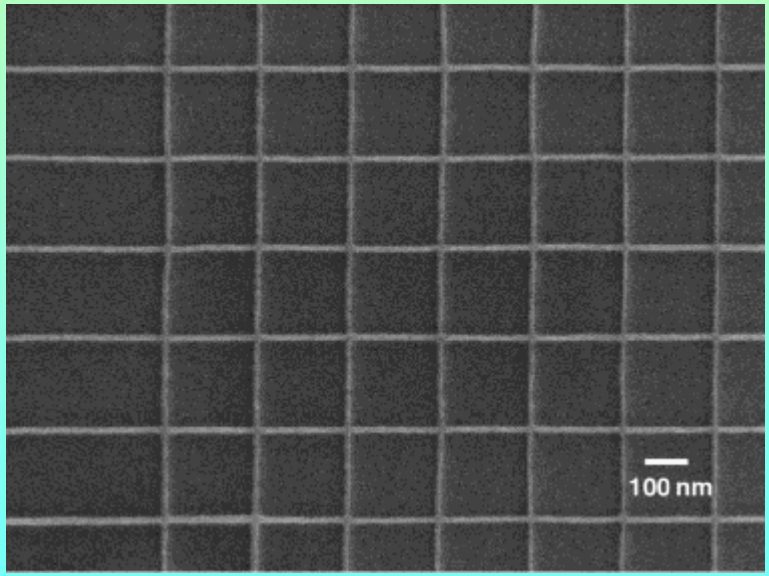
NTT Basic Research Laboratories

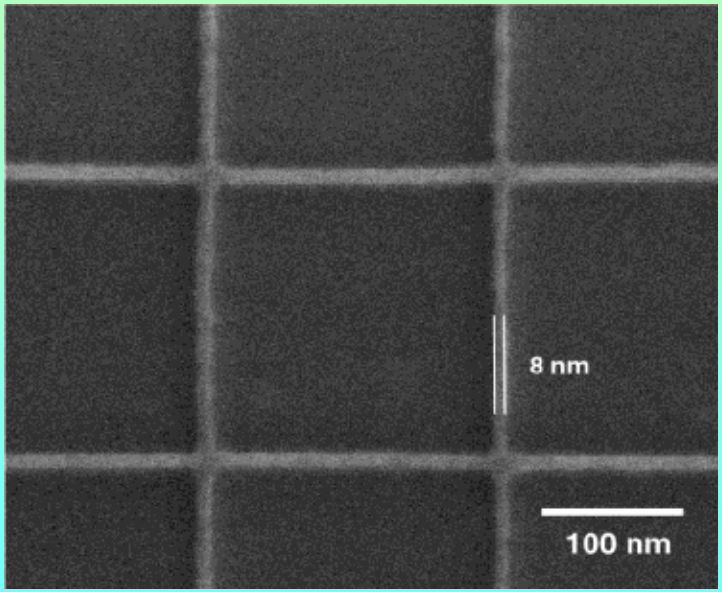
Sub-10 nm Electron Beam Nanolithography Using Spin Coatable TiO_2 Resists

University of Cambridge **and** *Leica Microsystems Lithography Limited*

Leica VB6-UHR-EWF 100keV

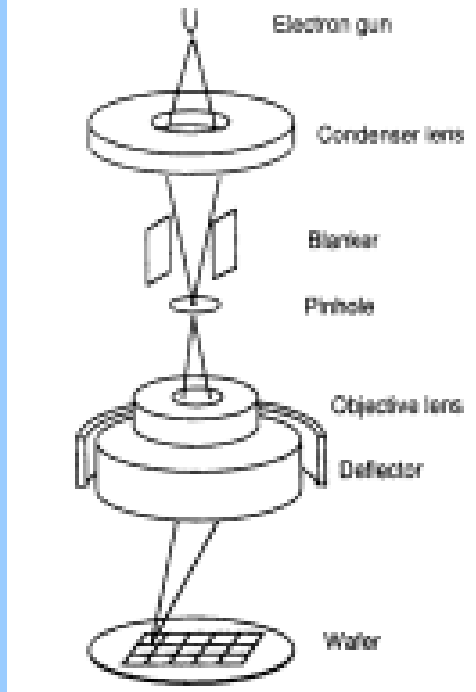
M. S. M. Saifullah,et al., Nano Letters, 3, 1587 (2003)



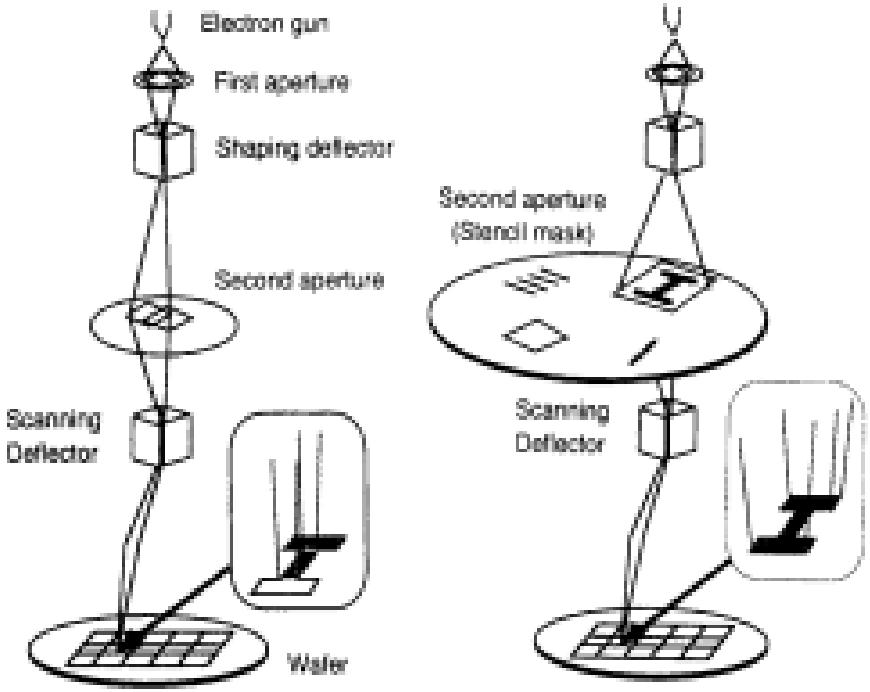


ＥＢ露光装置の用途と方式の違い

■研究開発用
スポットビーム方式



■半導体生産用
矩形成形ビーム方式と投影方式

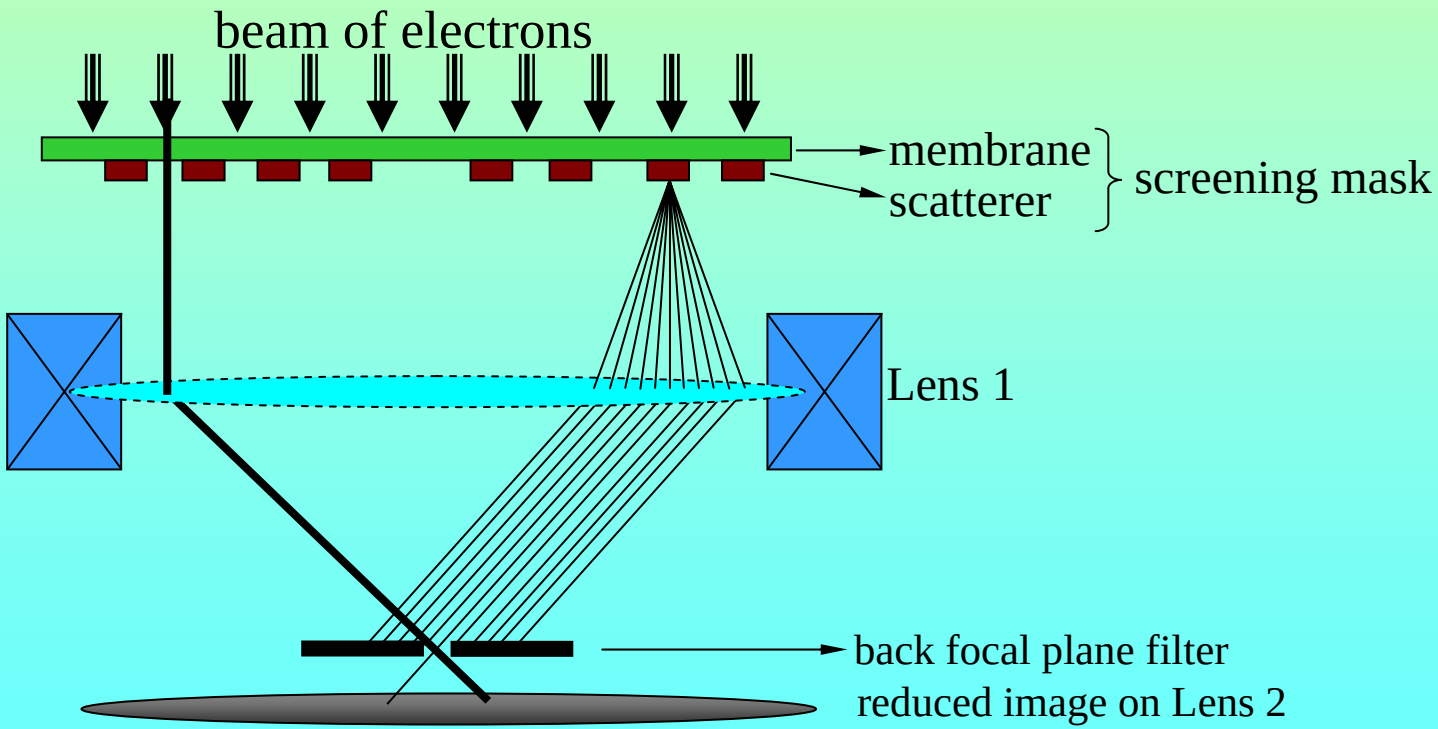


ELIONIX

- **Issues related to the integrated circuit industry:**
  - **Slow throughput**
    - A 0.1 μm diameter beam is < 10^{-12} the area of a 6” wafer.

Projection EBL Systems (SCALPEL):

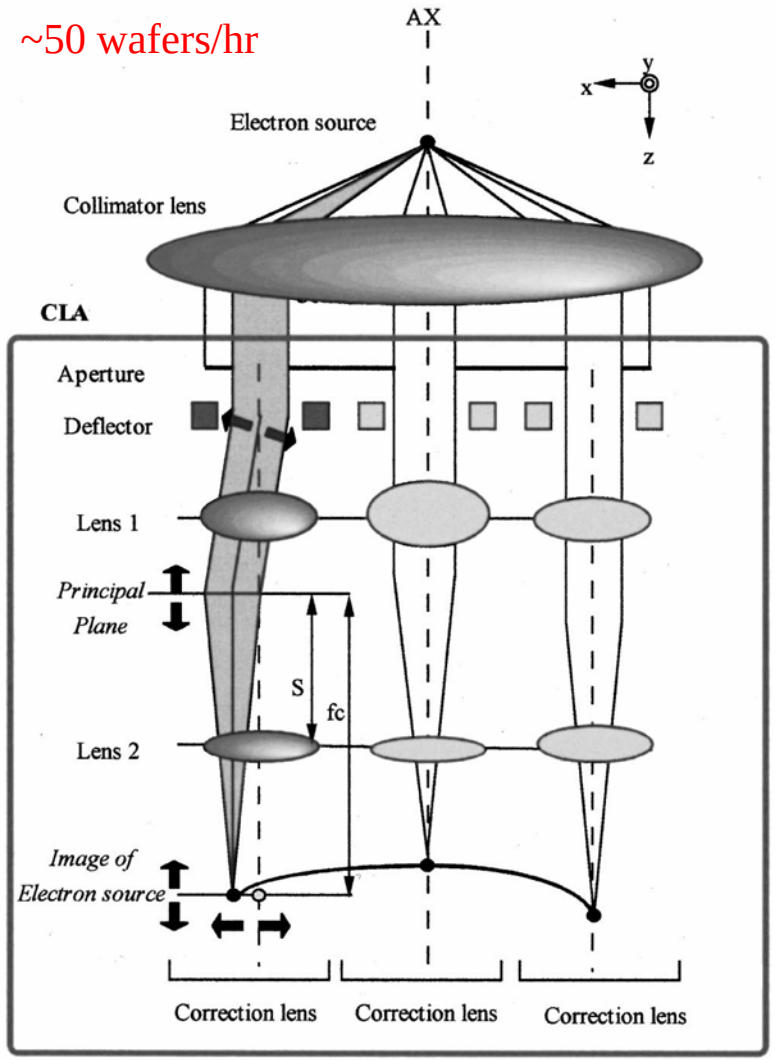
scattering with **a**ngular **l**imitation in **p**rojection **e**lectron beam **l**ithography



Multibeam direct-write electron beam lithography system

Single source with correction lens array

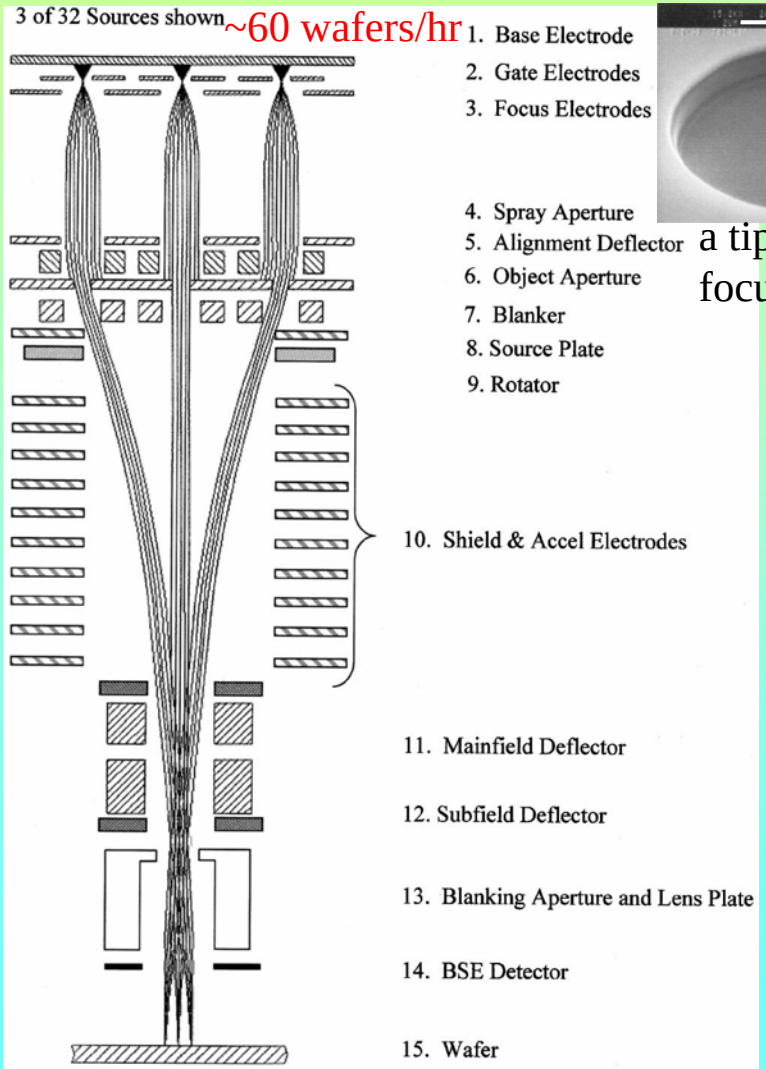
~50 wafers/hr

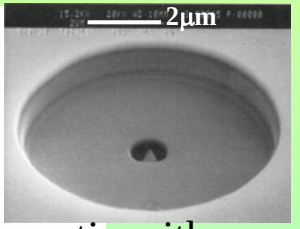


M. Muraki et al. J. Vac. Sci. Technol. B 18(6), 3061, 2000
Canon Inc.,

Multi-source with single electron optical column

3 of 32 Sources shown ~60 wafers/hr





a tip with focus electrode

E. Yin et al. J. Vac. Sci. Technol. B 18(6), 3126, 2000
Ion Diagnostics Incorporated

Take home message:

Extreme ultraviolet
electron beam projection } are considered leading contenders for next generation lithography

However, electron beam direct write system is a maskless lithography.

- **eliminating mask amortization costs and**
- **speed up chip development cycles.**

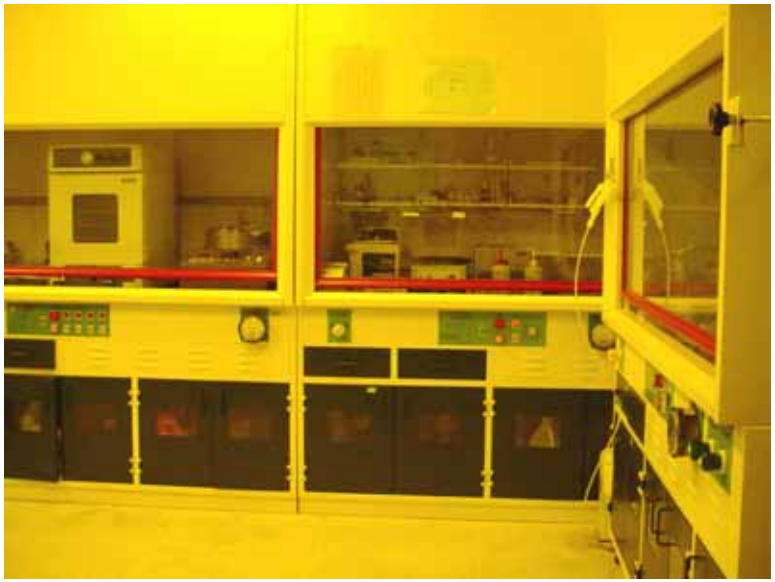
The ultimate resolution of electron beam lithography remains to be explored

Main applications:

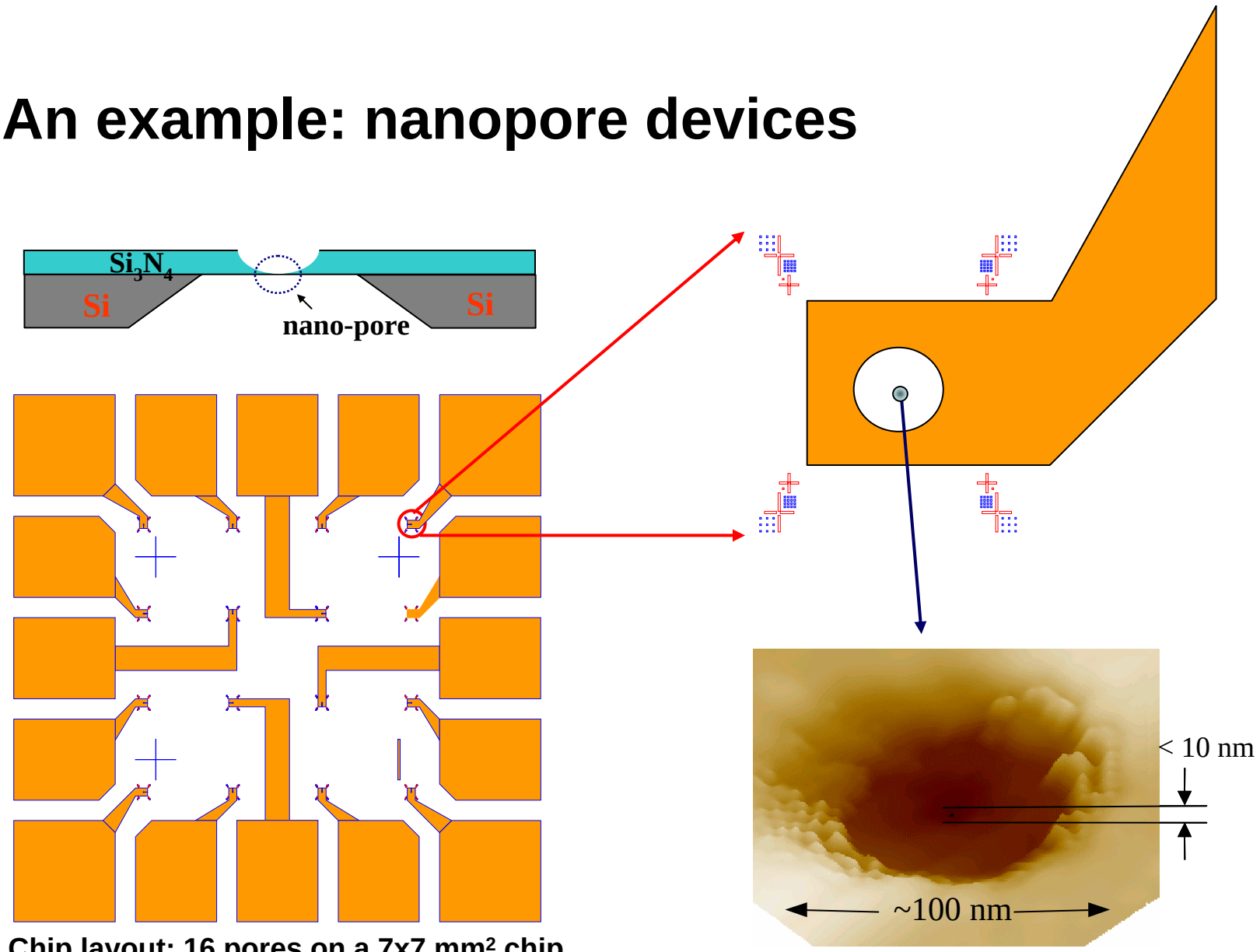
- **manufacture of small volume specialty products**
- **direct write for advanced prototyping of integrated circuits**
- **studies of quantum effects and other novel physics phenomena at very small dimensions**

How to make nanopore devices …

A full range of device fabrication facilities in a class-1000 cleanroom



An example: nanopore devices

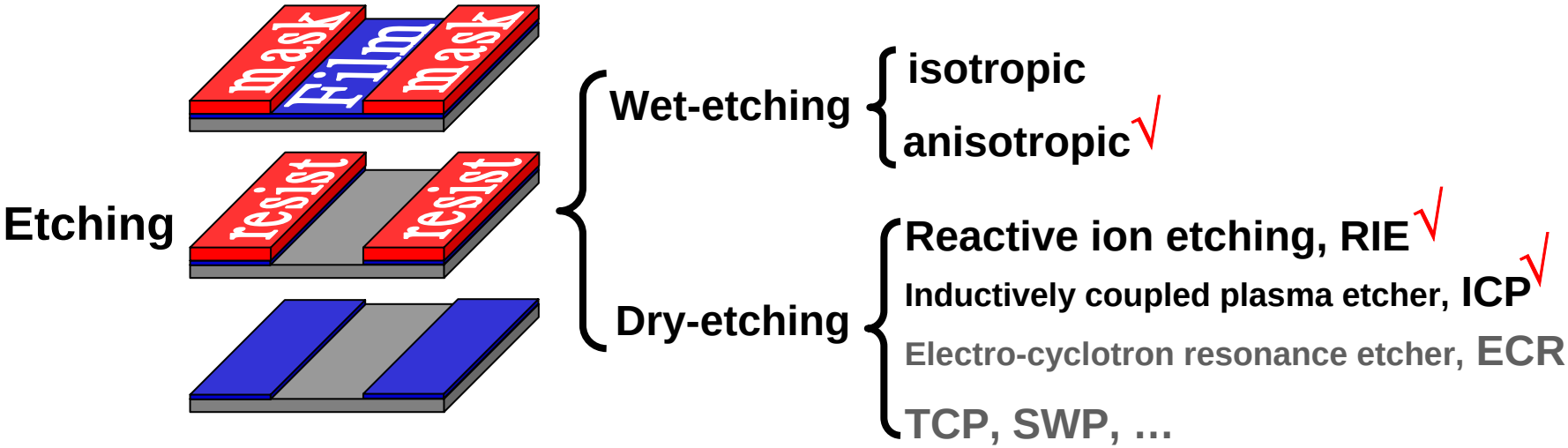


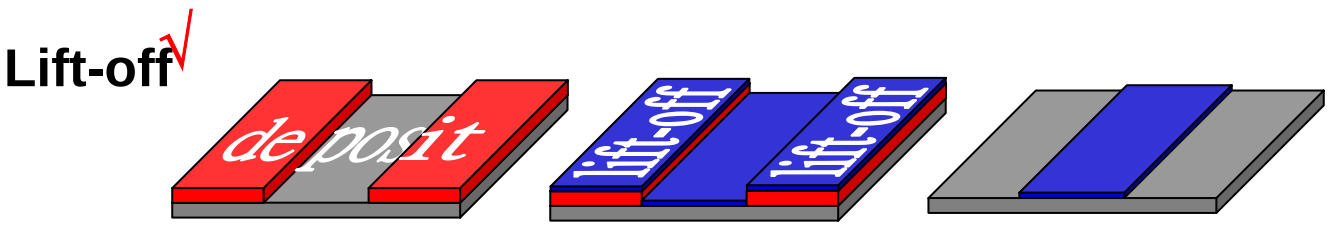
Chip layout: 16 pores on a 7x7 mm² chip

Lithographic process:

Deposition: Thermal evaporation, e-gun deposition, DC & RF sputtering,
Chemical vapor deposition (LPCVD, PECVD, APCVD)
Electrochemical deposition

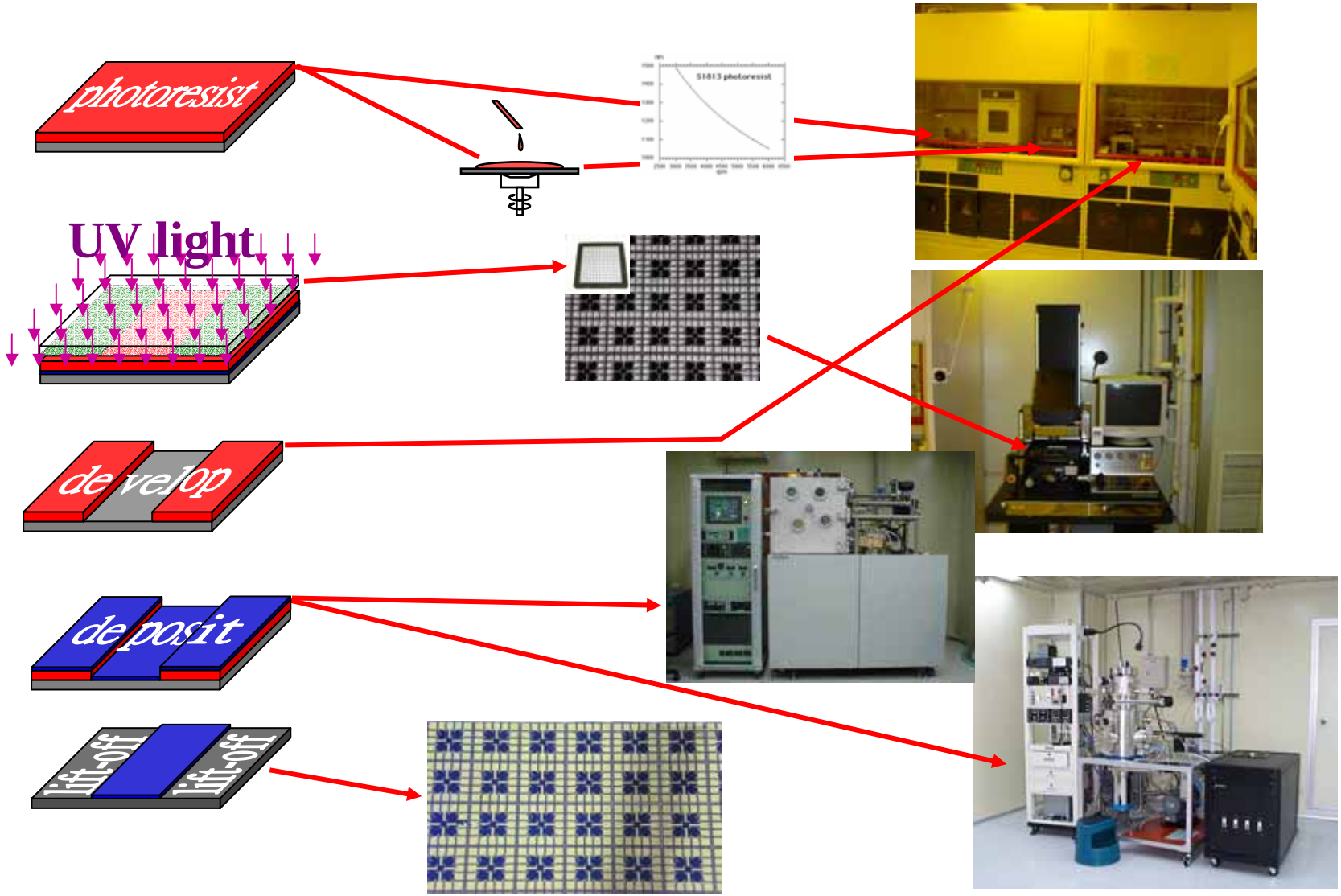
Patterning techniques:



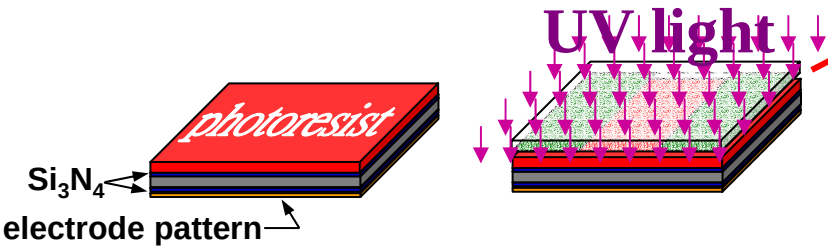


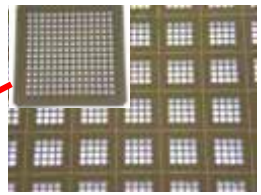
Step 1. LPCVD growth of Si_3N_4 (@NDL) on both sides of a 4'' Si-wafer

Step 2. Lift-off process for the top electrodes:

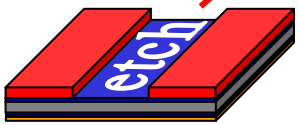


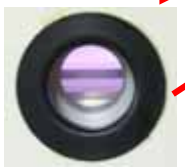
Step 3. Backside alignment

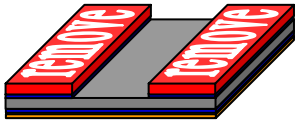


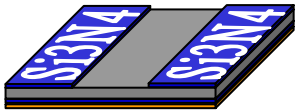


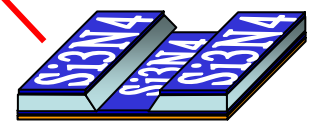
Step 4. RIE etching





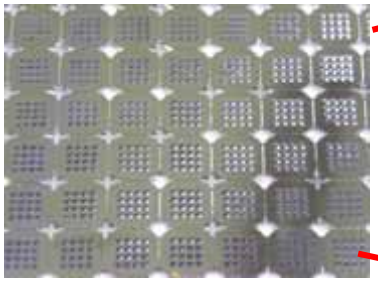


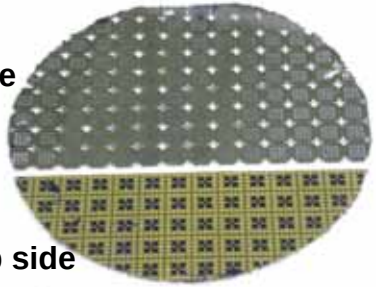


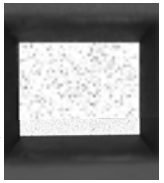


Step 5. wet etching

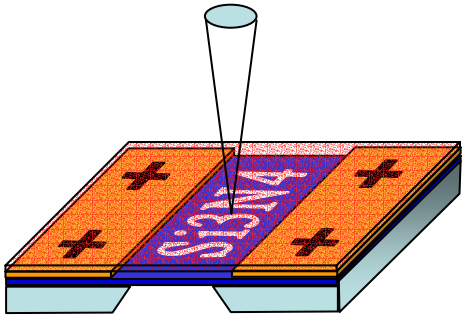
isotropic

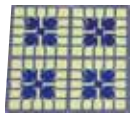


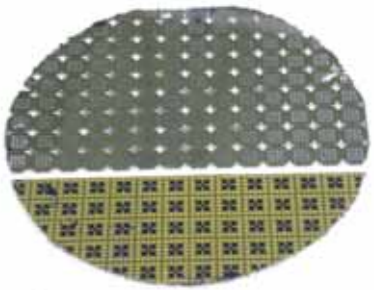




Step 6. e-beam exposure

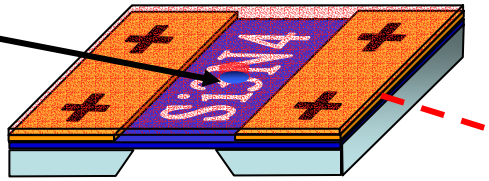




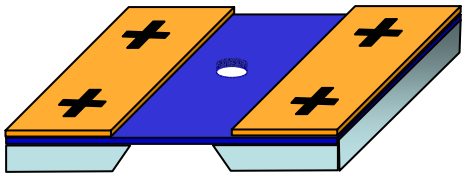


30keV

100keV



Step 7. RIE etching



Step 6 and 7 can be replaced by FIB etching,
but not for mass production

Step 8. counter electrode through metal mask

+

cover holder bottom holder

Process summary

Lift-off process

- A cleaner process
- Possible to achieve a smaller/narrower, better-defined shape
- Requires point evaporation source
- Requires undercut profile in resist mask
- Limited film thickness
- Only for low temperature process
- Problematic for structure with crystalline/high quality films

Etching process

- More flexible; compatible with high temperature deposition process
- Requires high-etching resistive and removable protection mask
- Potential risk with contamination left from protection mask
- Generally requires etching stop layer
- Edge roughness due to thickness in variation etching mask

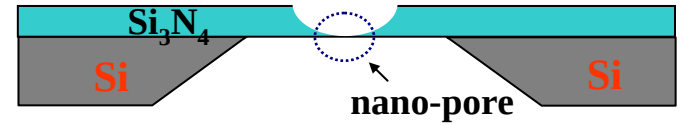
Wet etching:

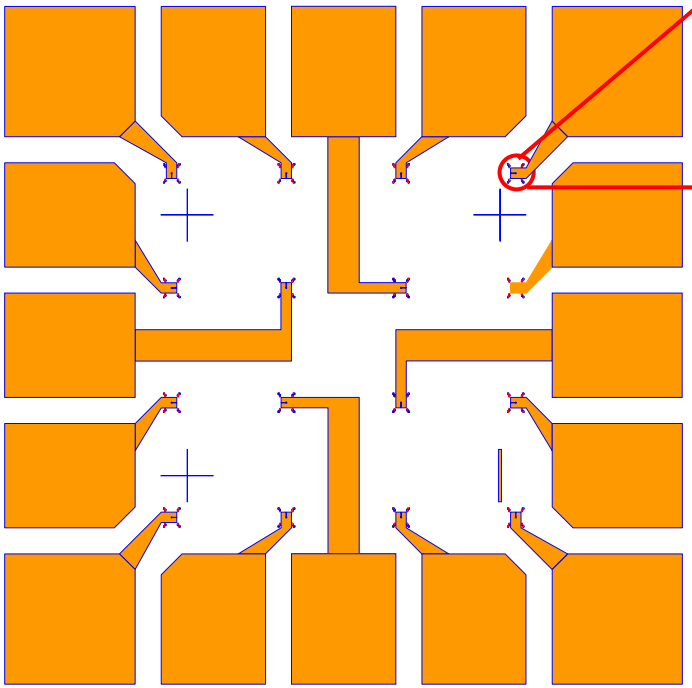
- No expensive equipment required
- Potential source of pollution from various etching solutions
- Contamination from etching/rinse solution
- Require good mask-layer adhesion
- Undercut profile for isotropic etching

Dry etching:

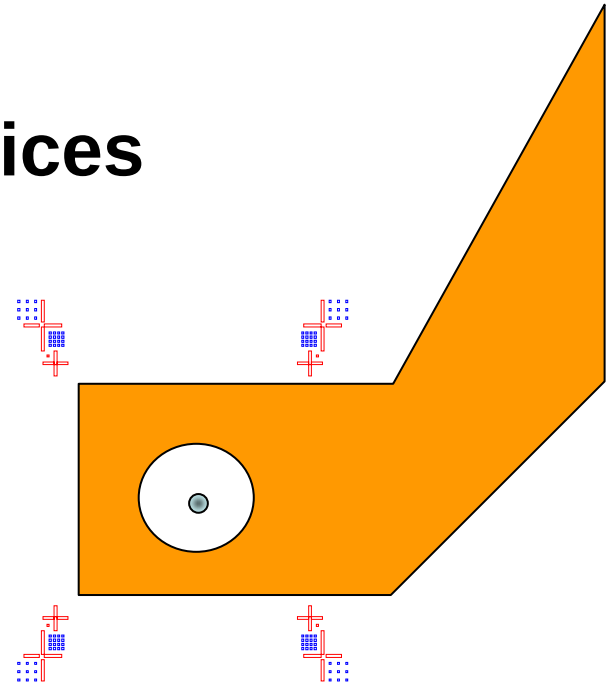
- Less contamination

An example: nanopore devices

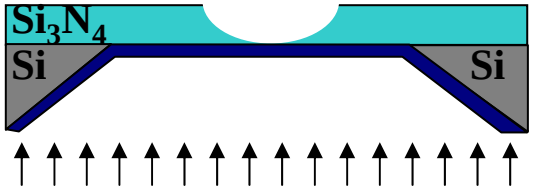




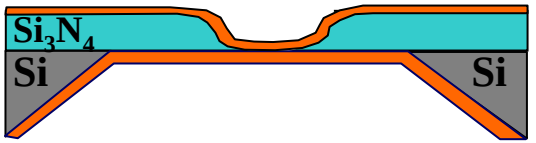
Chip layout: 16 pores on a 7x7 mm² chip



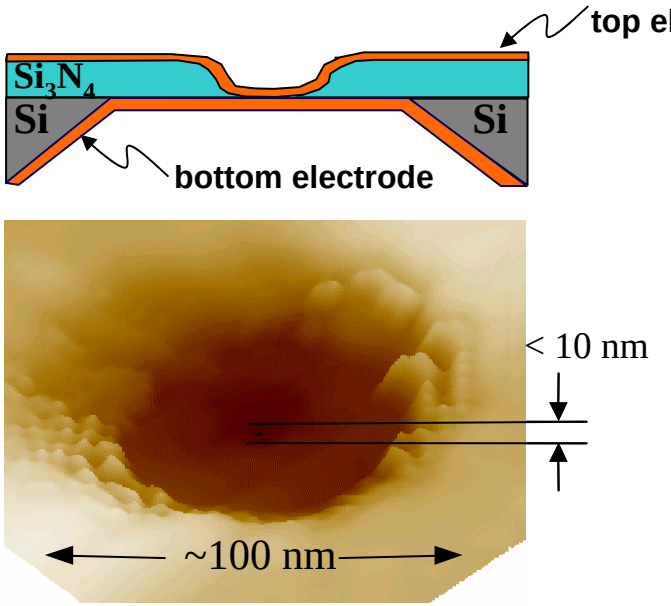
Deposition of bottom electrode



Deposition of molecules and top electrode

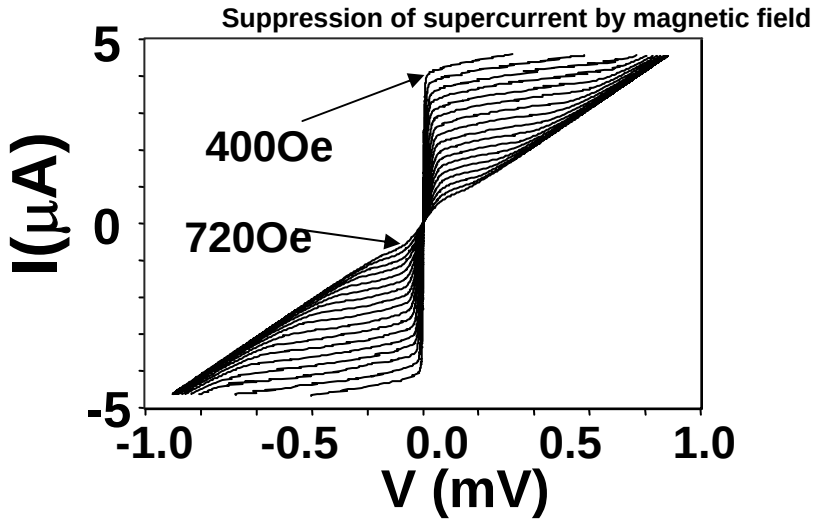


Nanopore electronics

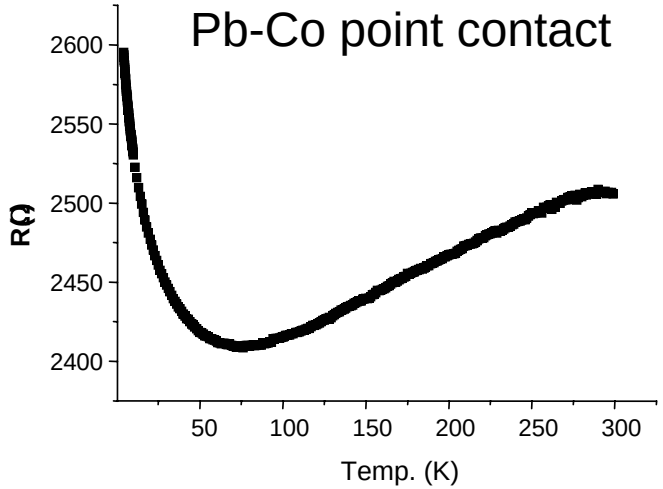


Al-Al superconducting point contact

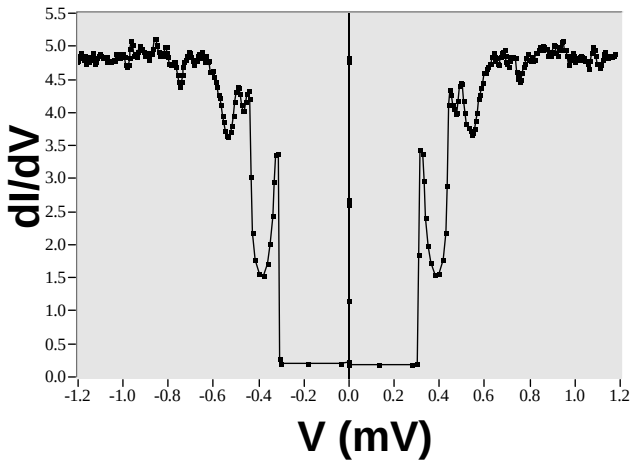
Al-Al superconducting point contact



Pb-Co point contact



Multiple Andreev Refelection

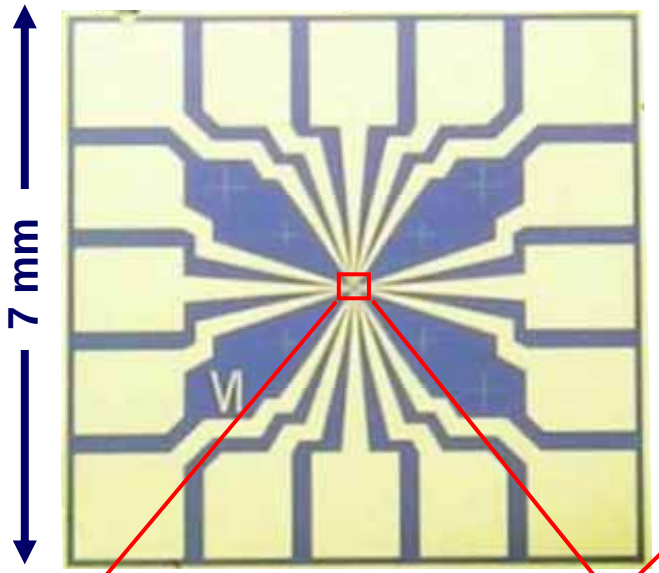


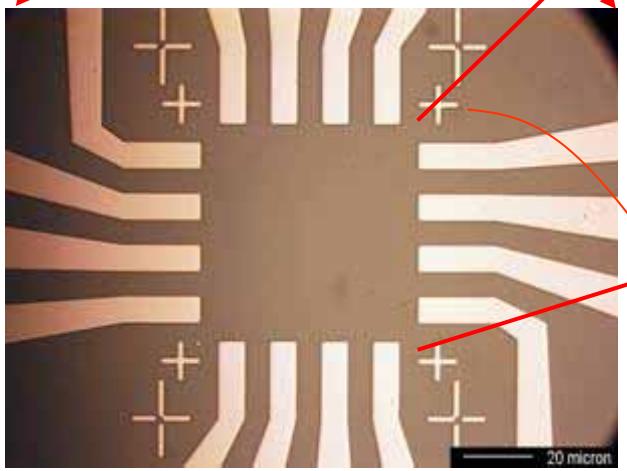
Sample fabrication: Core facilities at Academia Sinica

Measurement equipment

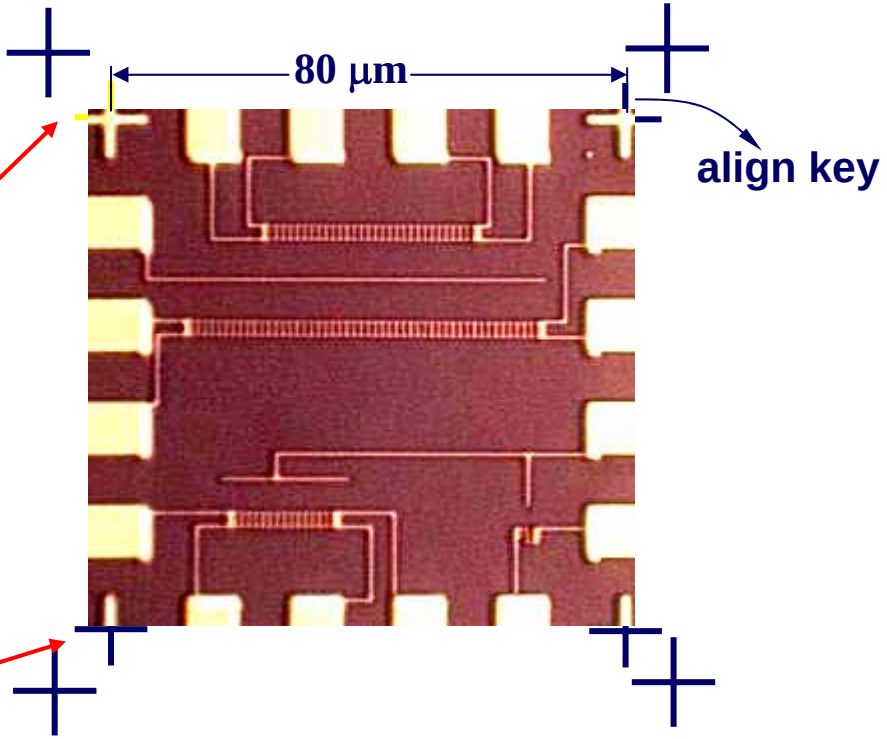
Mix and Match technology

Photolithography



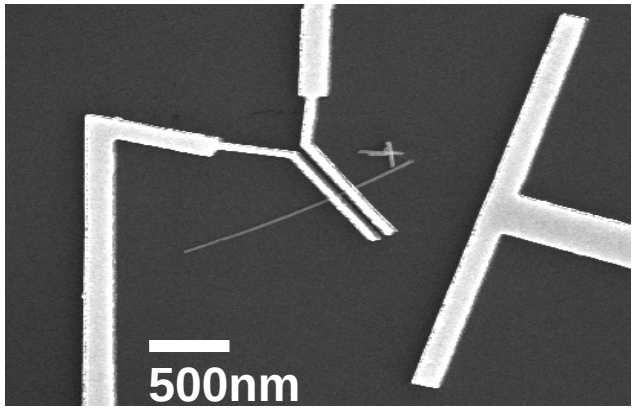


e-beam lithography

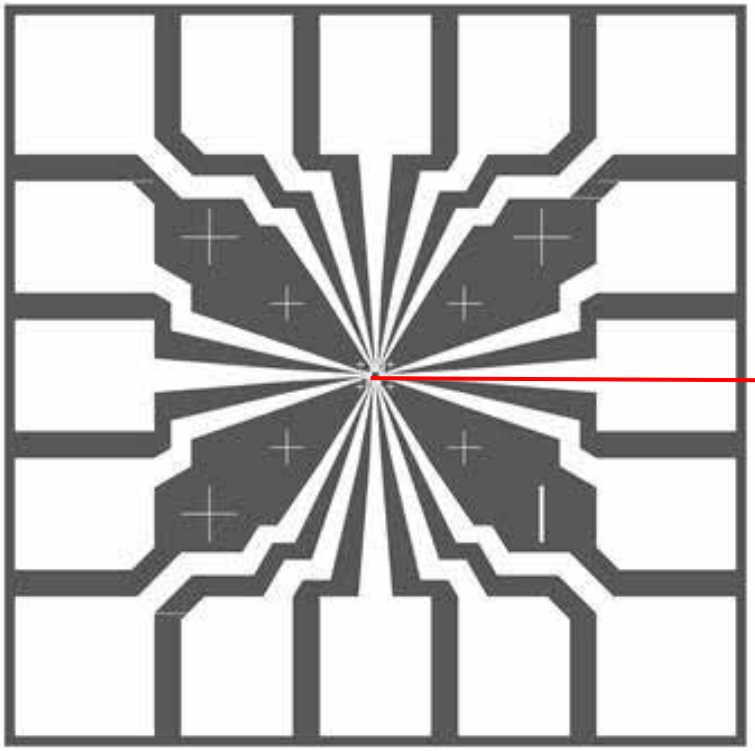


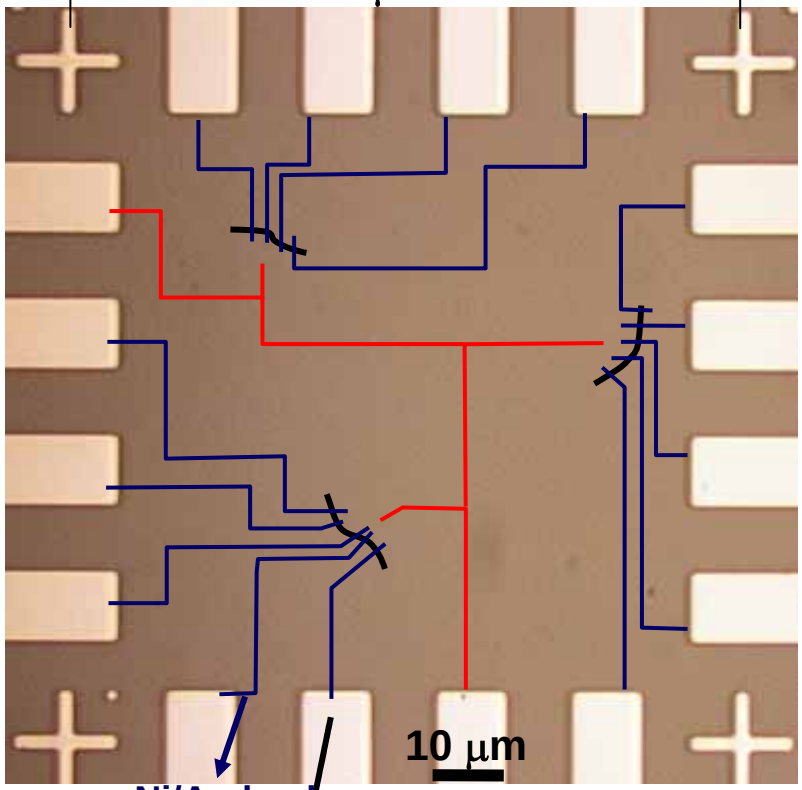
align key

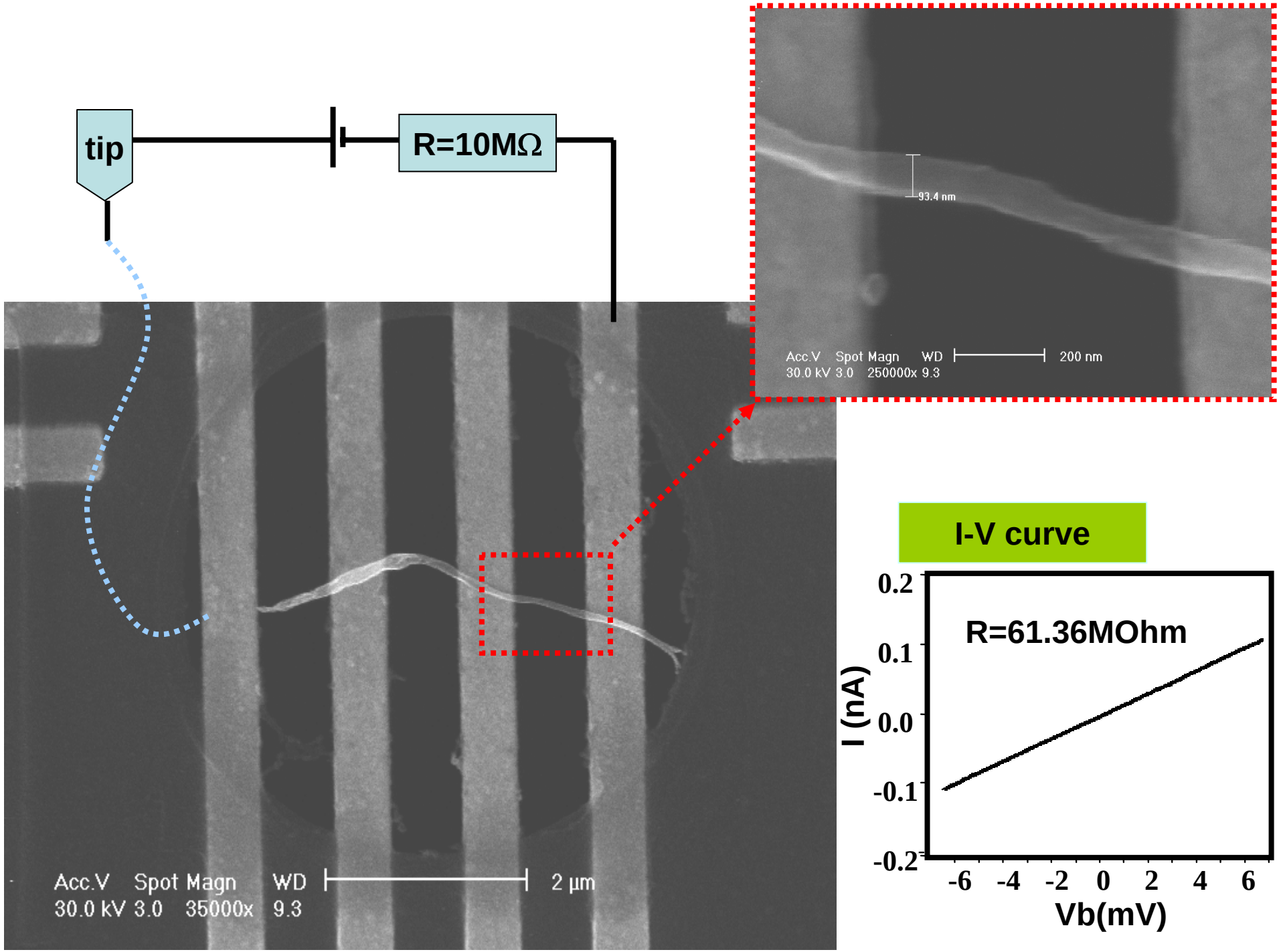
Device fabrication



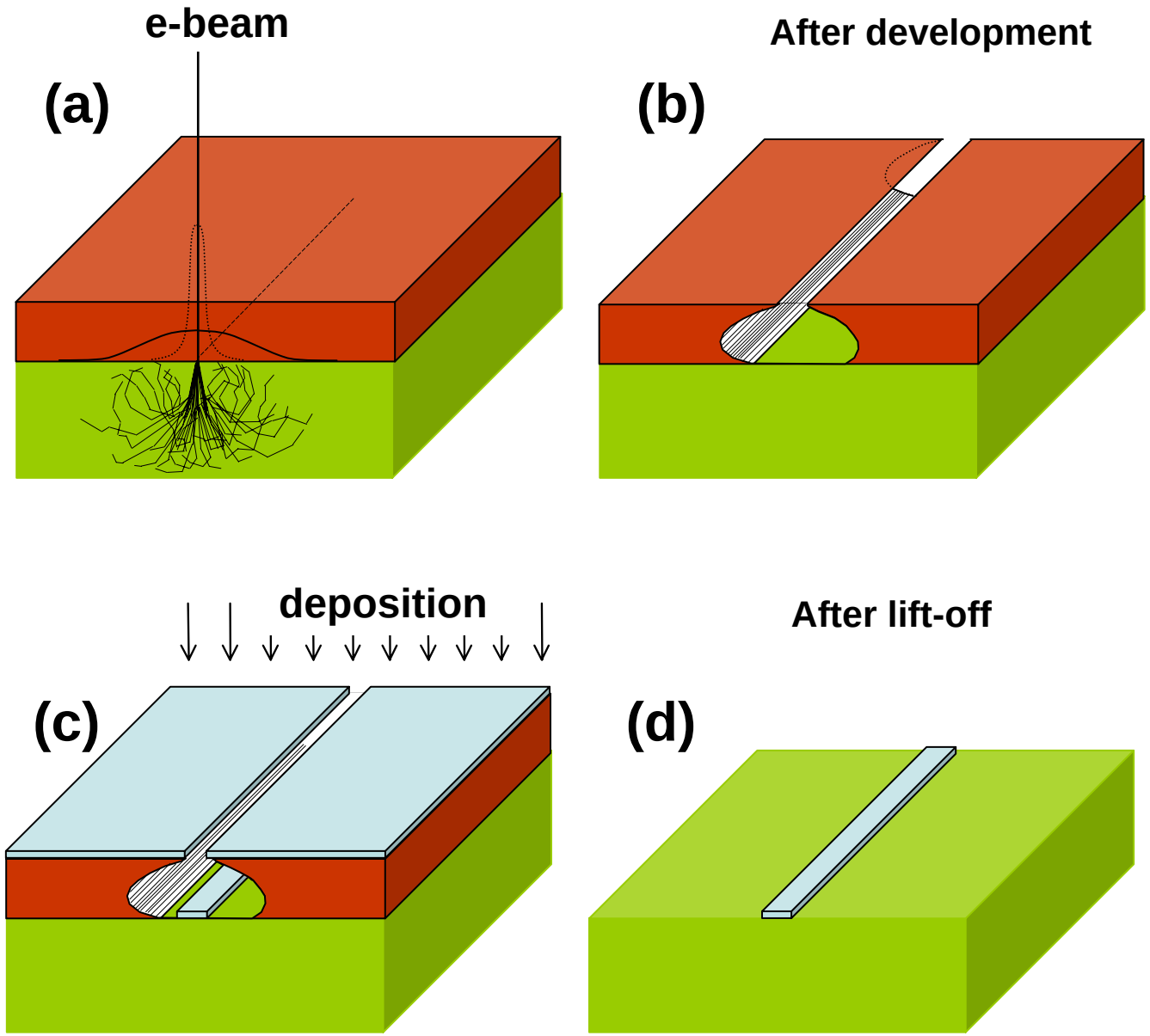
Chip layout





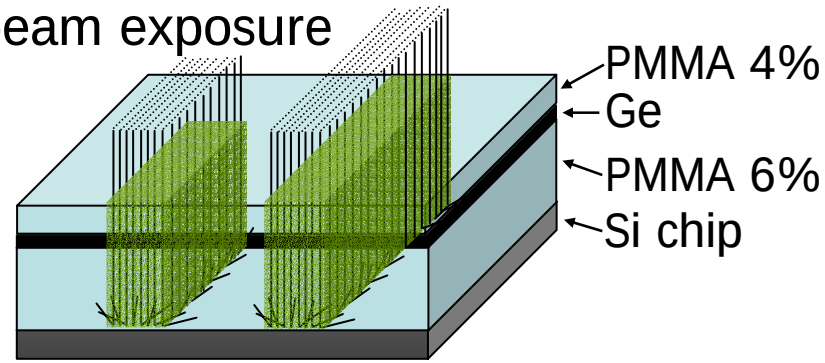

tip
R=10MΩ
93.4 nm
Acc.V Spot Magn WD 200 nm
30.0 kV 3.0 250000x 9.3
Acc.V Spot Magn WD 2 µm
30.0 kV 3.0 35000x 9.3
I-V curve
R=61.36MOhm
I (nA)
0.2
0.1
0.0
-0.1
-0.2
-6 -4 -2 0 2 4 6
Vb(mV)

E-beam lithography for nano-scaled electrodes

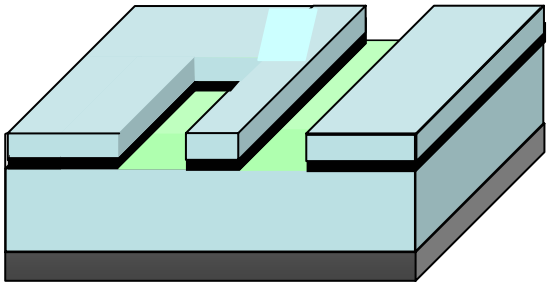


Fabrication of Aluminum tunnel junctions

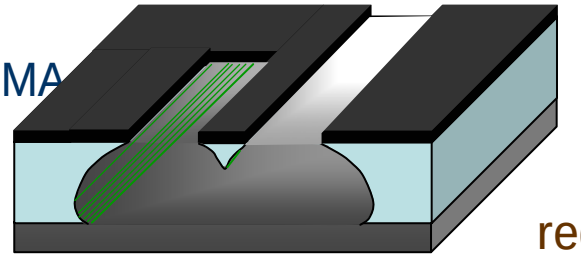
1. e-beam exposure



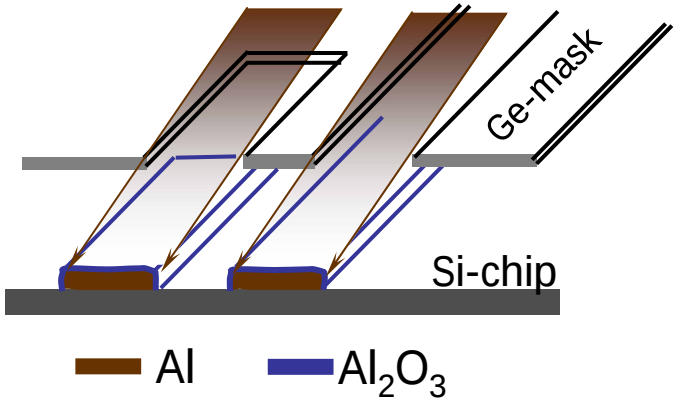
2. development and Ge-etching



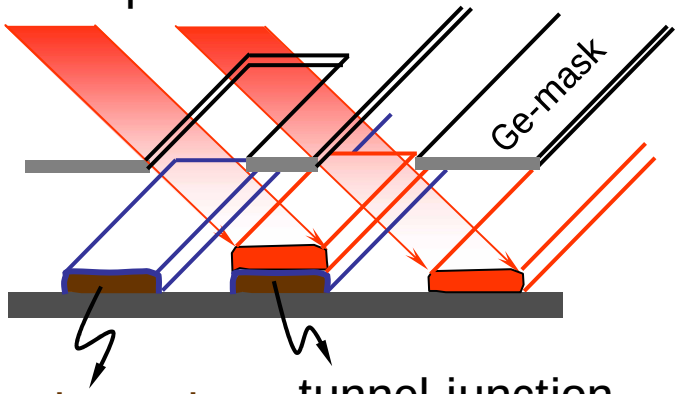
3. O_2 dry etching of the bottom PMMA



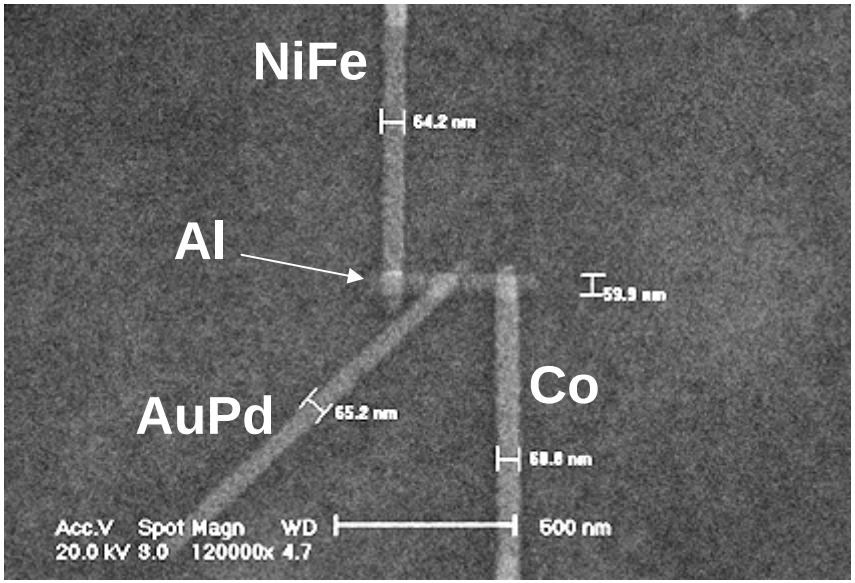
4. Al- evaporation + oxidation

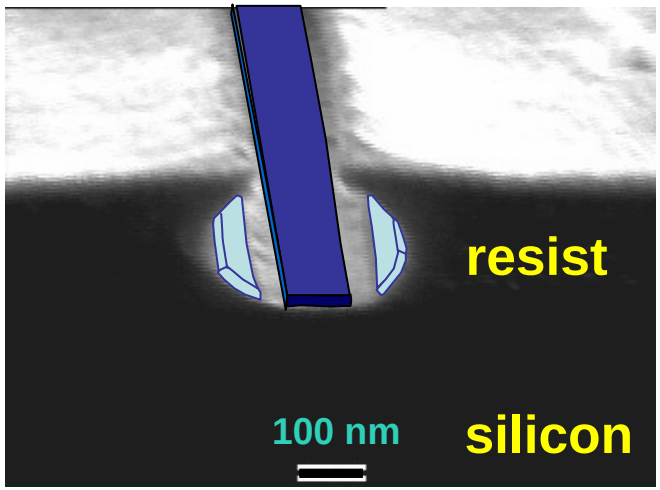


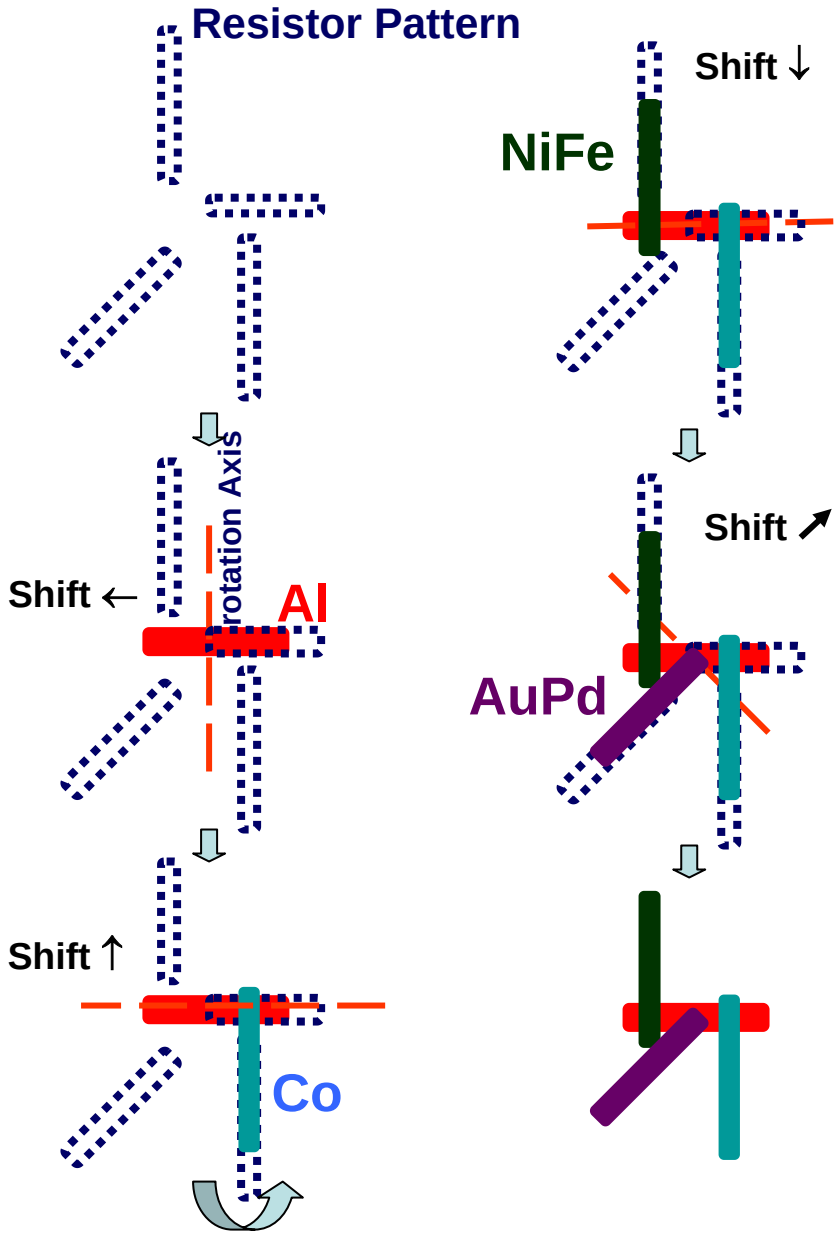
5. evaporation of counter electrode



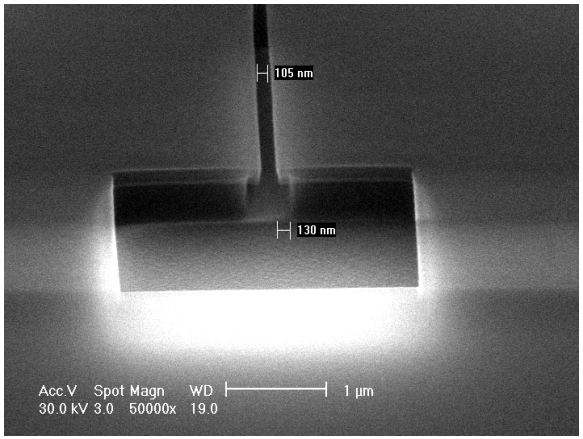
Multiple angle evaporations

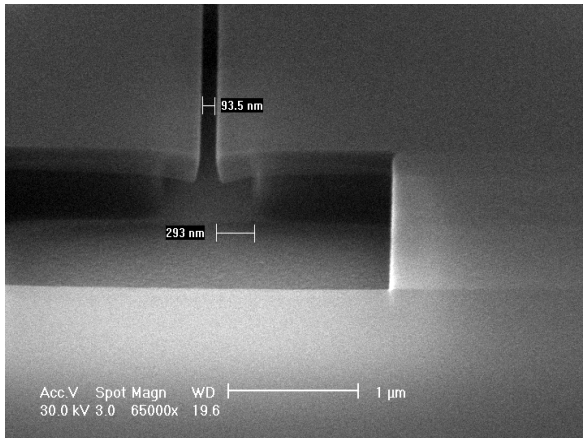


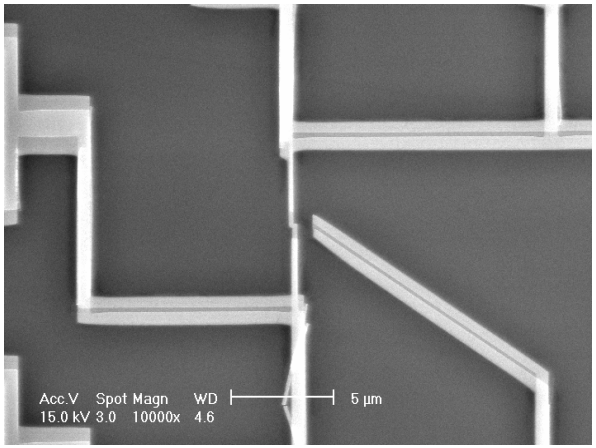


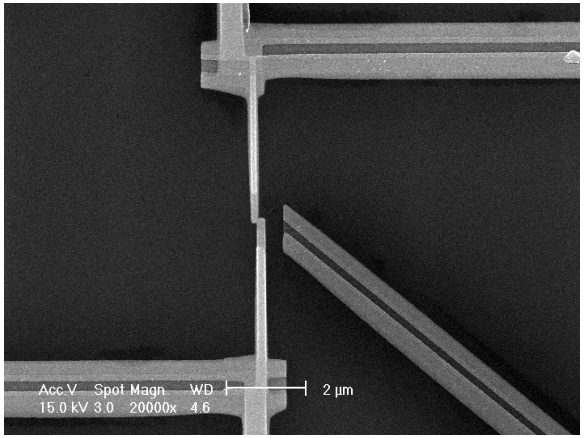


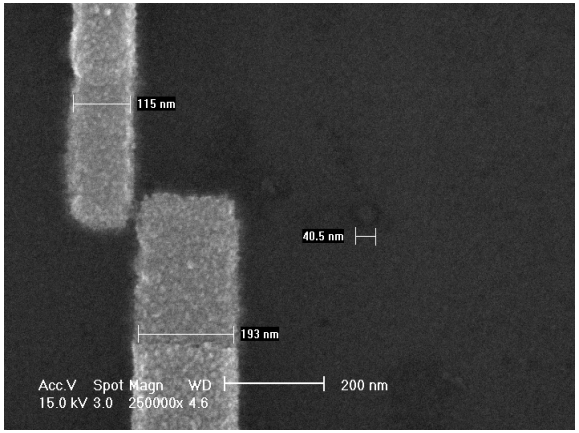
Fabrication of small-dot Ferromagnetic single electron transistors





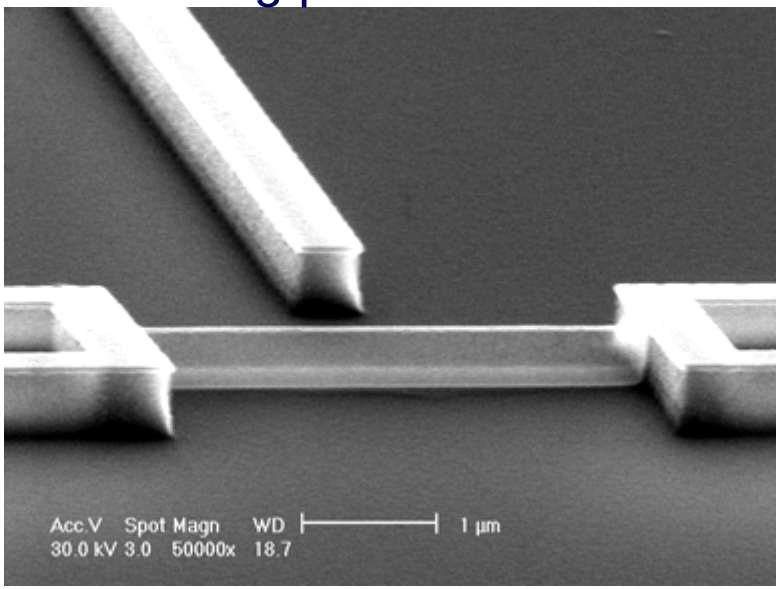




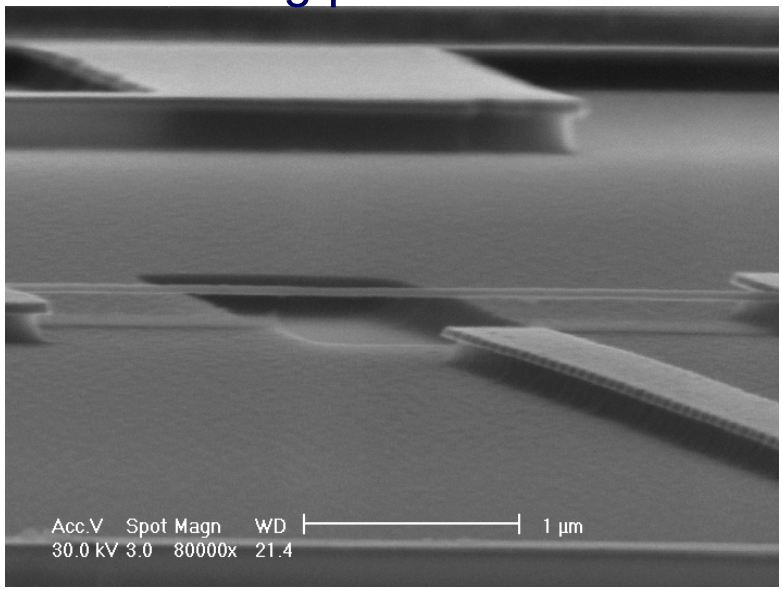


Dry etching vs. isotropic wet-etching

ICP etching profile

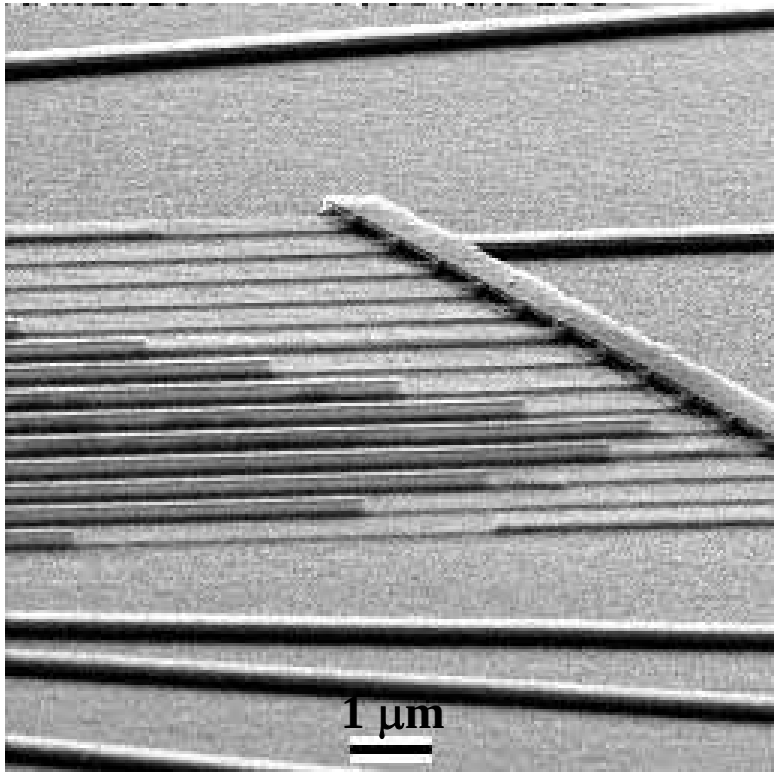


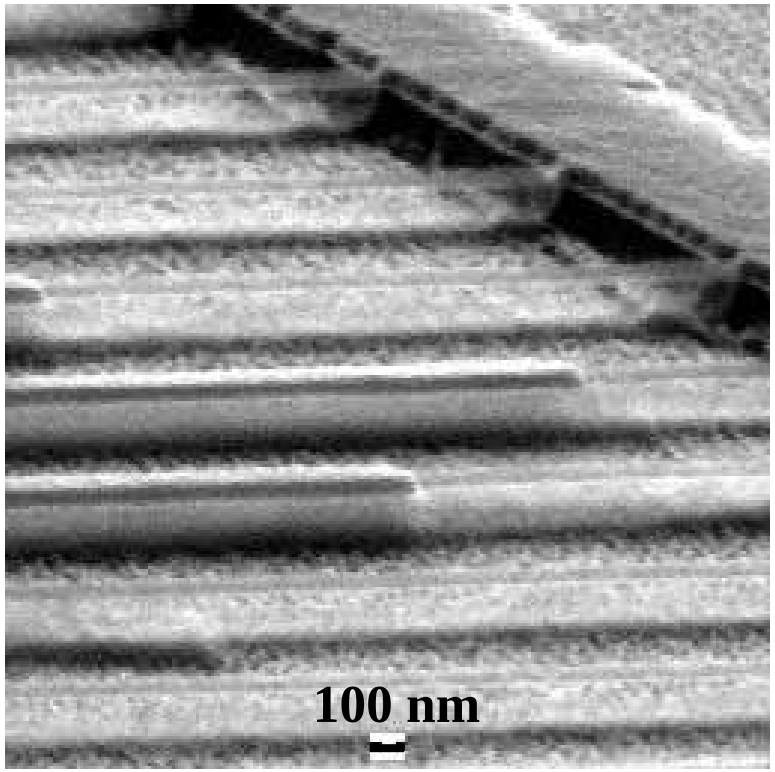
Wet etching profile



40nm-wide suspending Cr wires

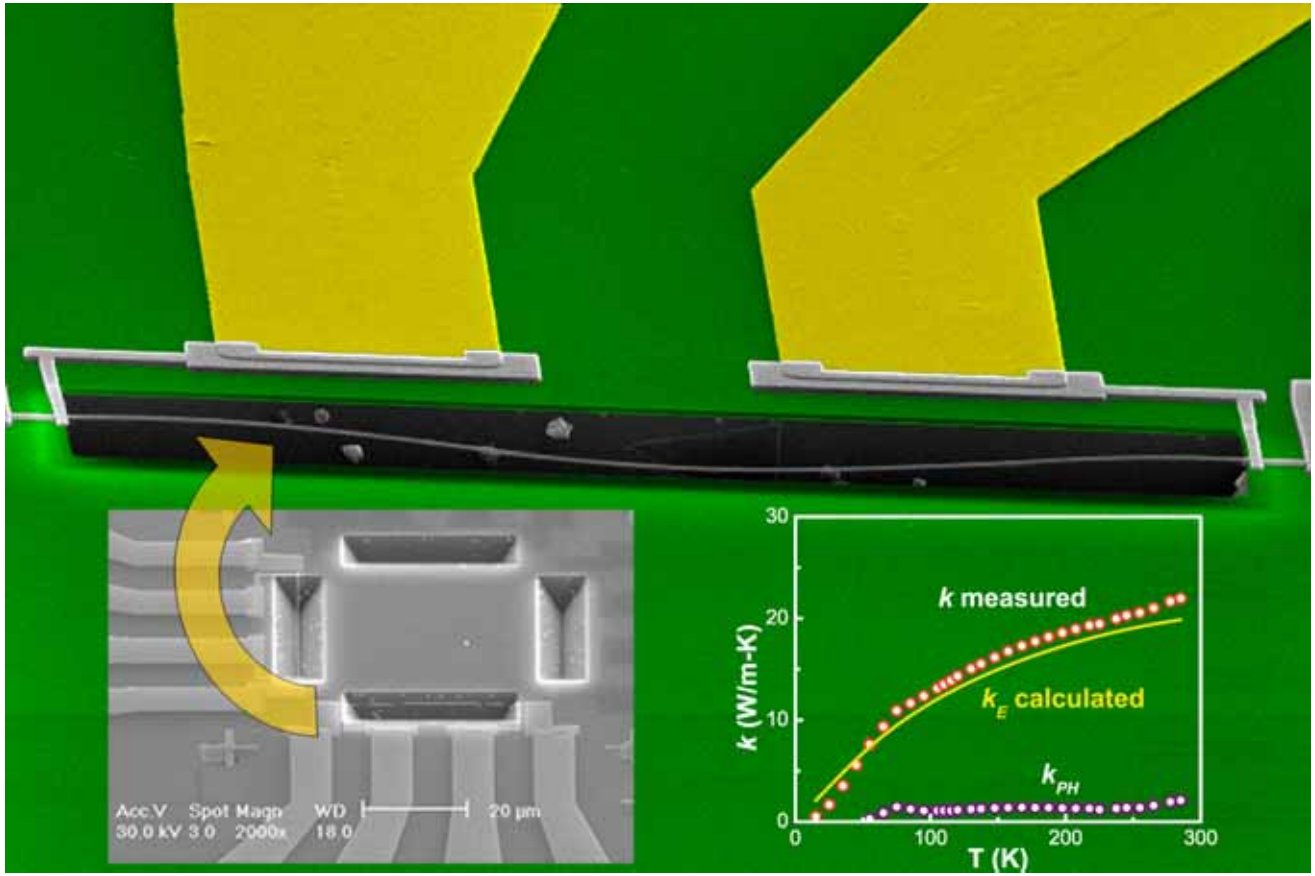
made on SOI substrates





Electrical and thermal transport in single nickel nanowire

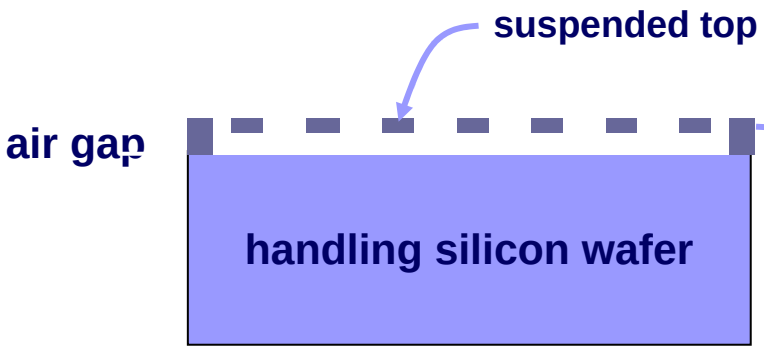
M. N. Ou1,（歐敏男）, T. J. Yang（楊宗哲）, S. R. Harutyunyan,
Y. Y. Chen（陳洋元）, C. D. Chen（陳啓東）, S. J. Lai（賴水金）

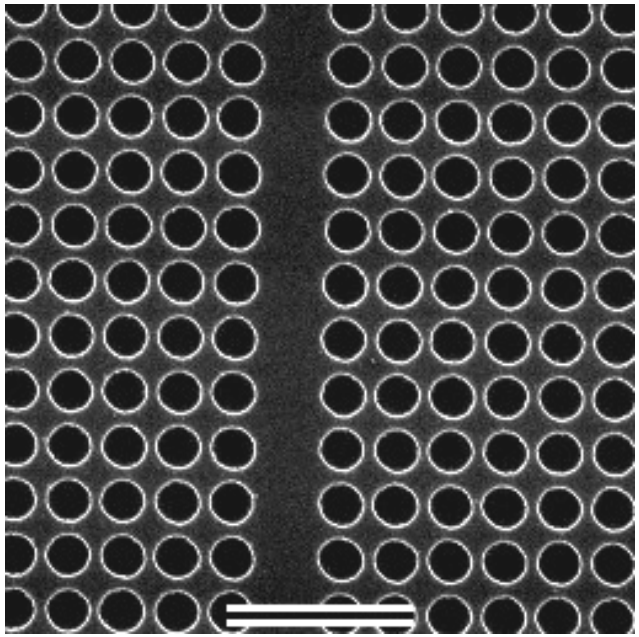


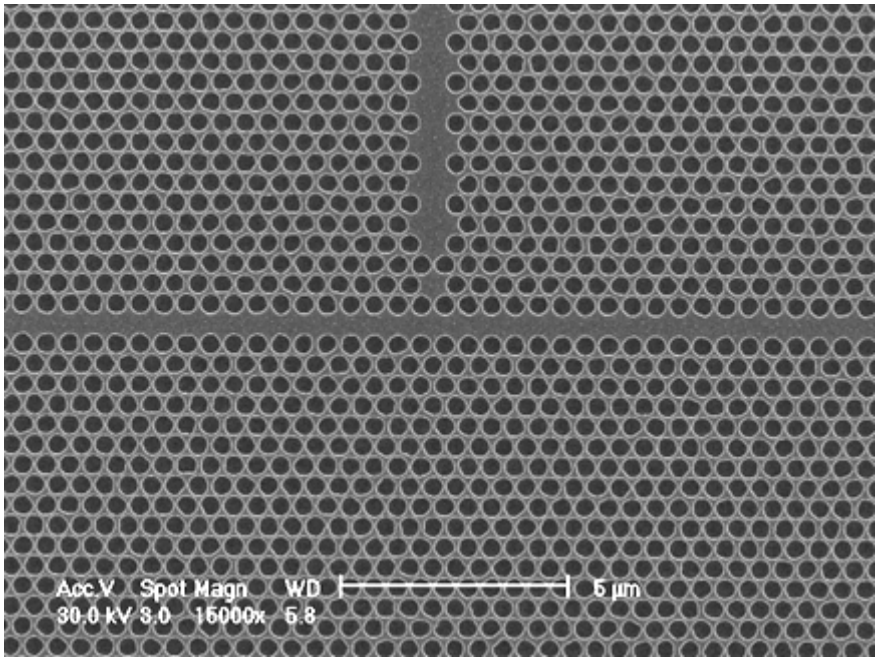
appeared as the cover of APL January 2008 issue

SON (silicon-on-nothing) photonic crystal

made on SOI (Silicon On Insulator) wafer

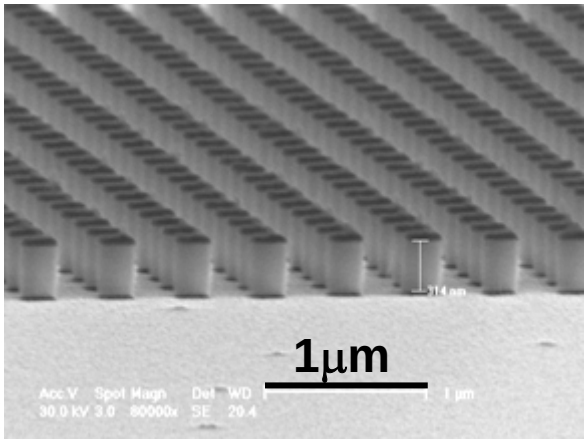




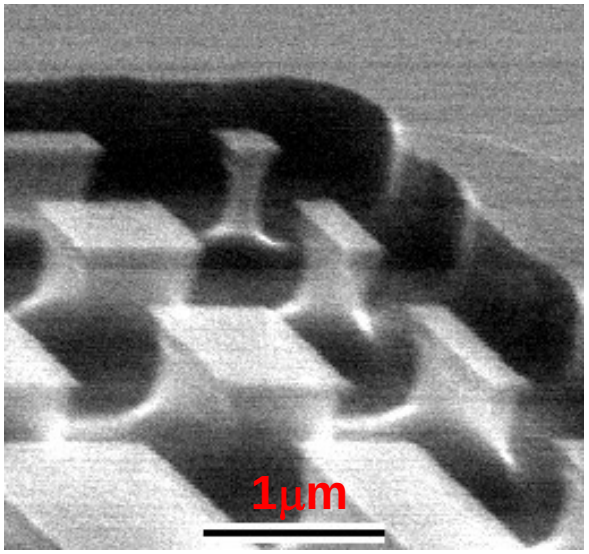


Diameter~220nm Pitch ~310nm

Comparison between RIE and ICP etching

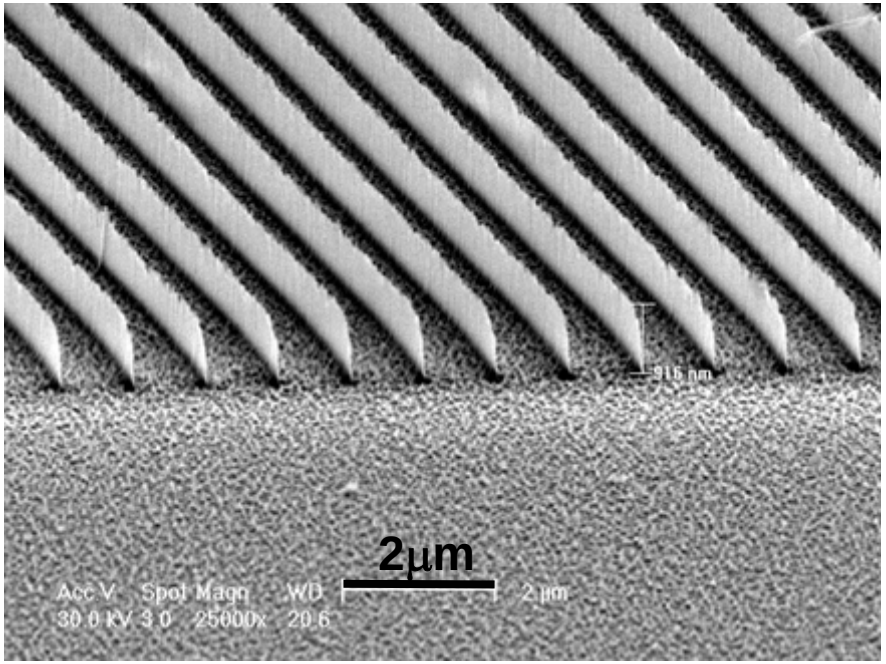


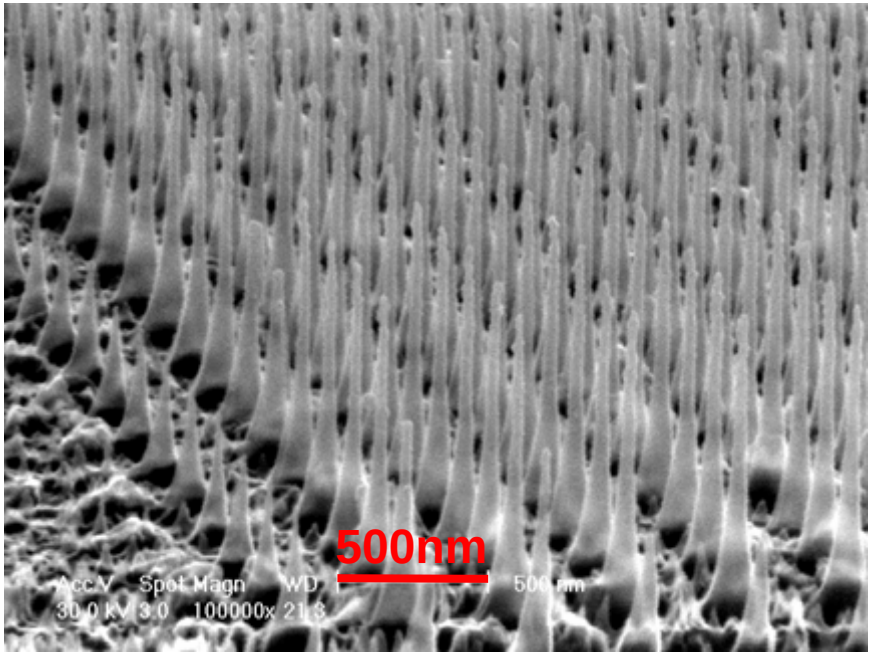
For directional etching
Etching Si-base materials
C_4F_8, SF_6, Ar, O_2



For undirectional etching
Etching Si-base materials
and some metals
CF_4, Ar, O_2

Quartz Molds for Nano-imprinting



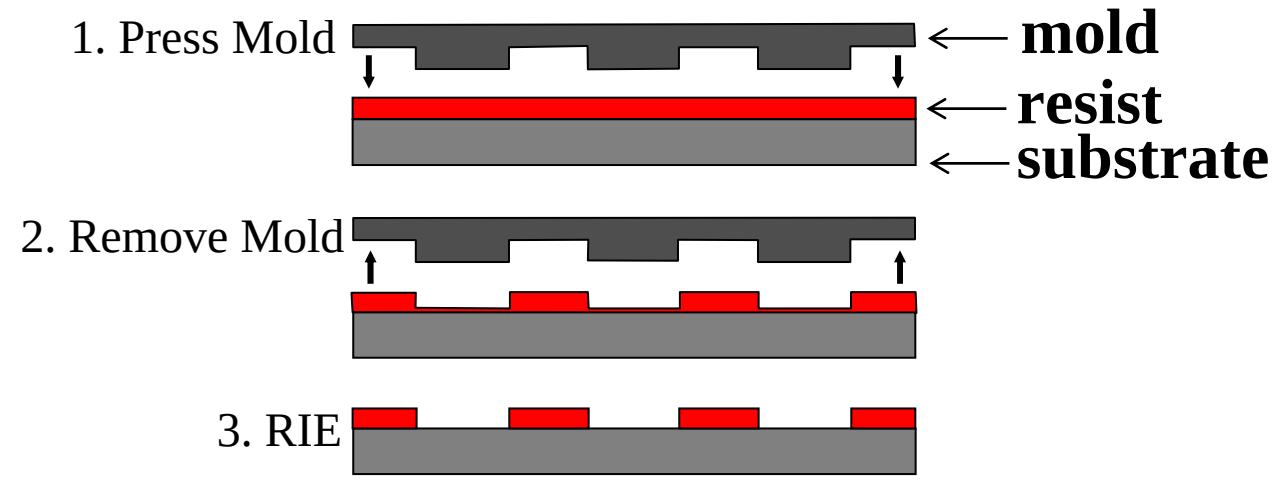


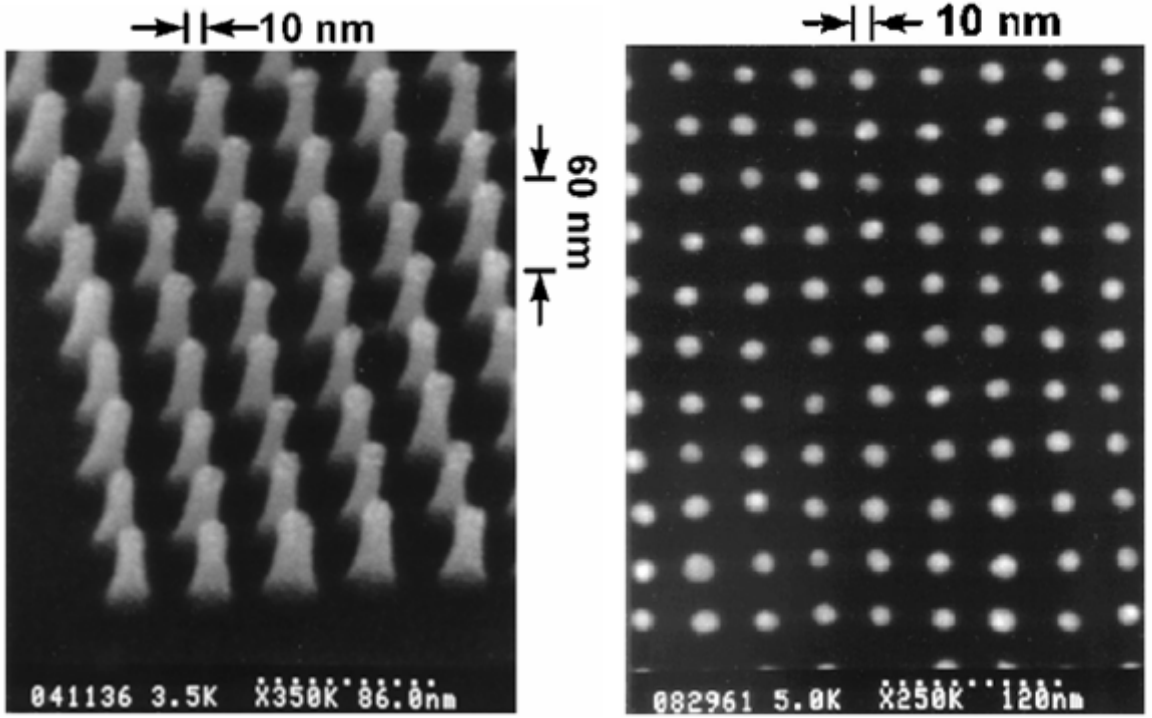
ICP-RIE recipe:

Ar/C_4F_8 power 700W bias 50V

etching time:300sec

nanomolds for imprint lithography



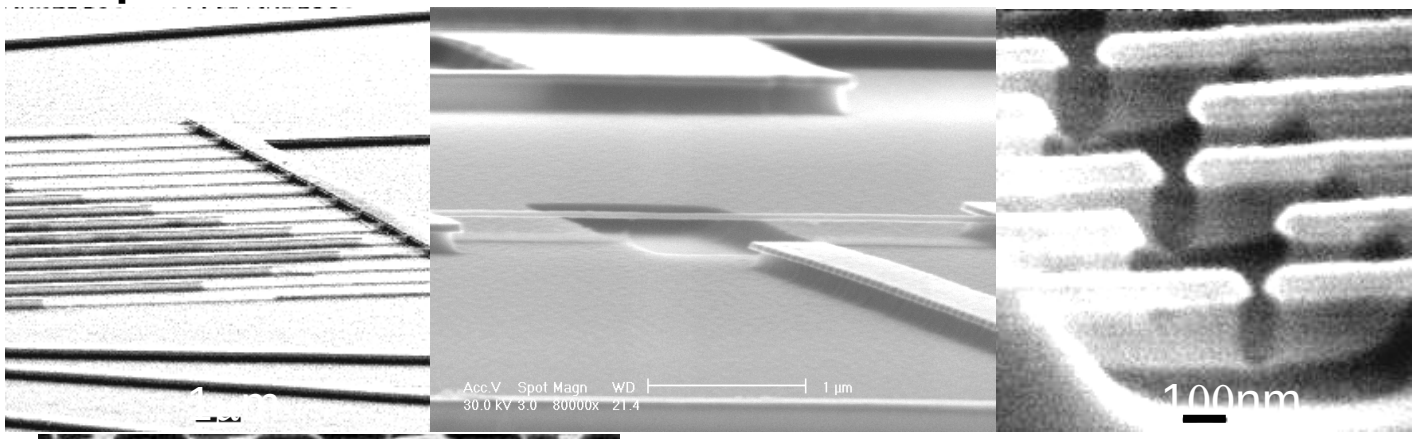


Stephen Y. Chou et al.

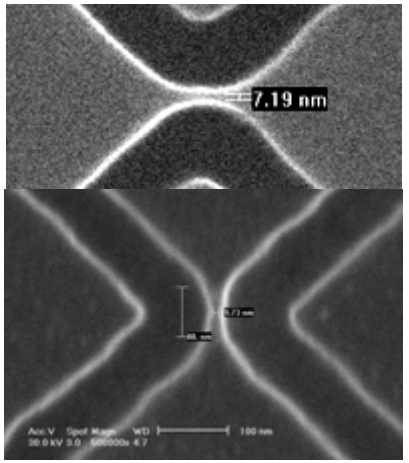
J. Vac. Sci. Technol. B, 15(6), 2897 (1997)

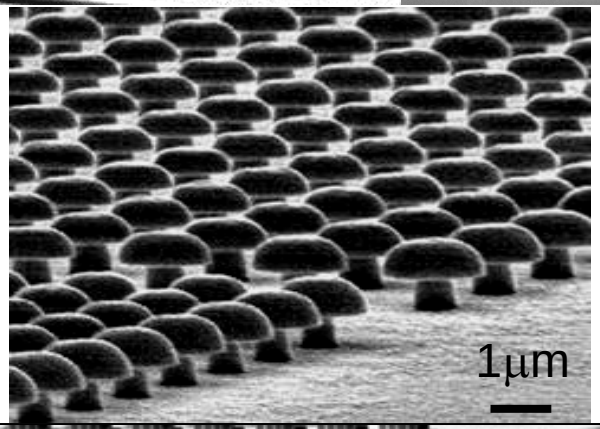
Tricks and Know-how

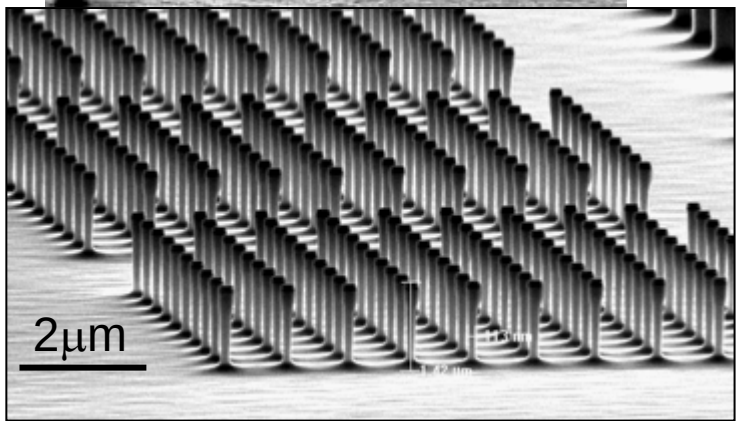
Suspended wires



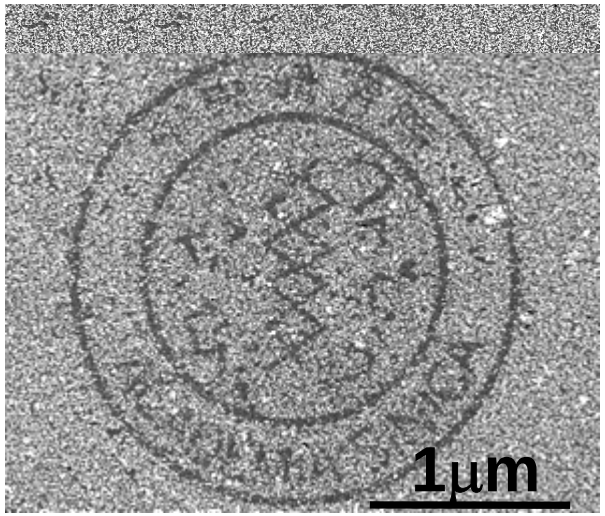
sub 10-nm Si-wires

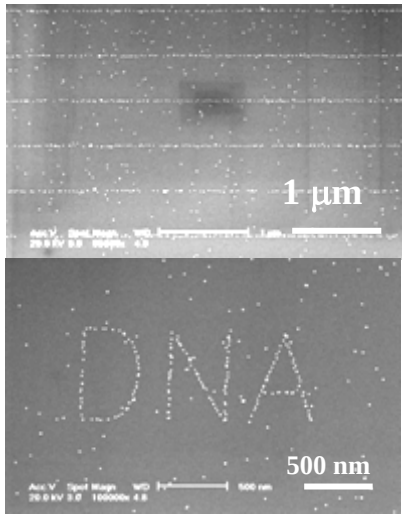






DNA-mediated Au-particle patterning techniques





Rule of thumb

1. **Minimize number of process steps**
2. **Minimize number of masks: use self-alignment whenever possible**
3. **Use wafer-stage process whenever possible**
4. **Use lift-off instead of etching if possible**
5. **Use positive resist instead of negative resist if possible**
6. **If a recipe works, don’t mess it up**

Main messages:

1. **Lithography is an art with know-how, experience and tricks**
2. **Needs to play around with resist profile and material issues**

Nano devices:

Play with fabrication technology

Explore emerging physics

Look for new applications