Advanced Device Fabrication Techniques

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Outline:

1 State-of-the-art device fabrication techniques
   Future light sources: EUV and e-beam

2 e-beam lithography

3 Examples:
   nano-pore based point contact devices
   nano electronic devices
Lithography = Pattern transferring
Standard etching process

- substrate
- coated film
- photoresist
- UV light
- mask plate
- CVD, Thermal, e-gun, Sputtering, spin-coating
- develop
- etch
- remove exposed part (for positive-tone PR)
- selective dry/wet etching
- remove resist mask
- finished pattern
Complementary process: lift-off

- develop: remove exposed part (for positive-tone PR)
- deposit: Thermal, e-gun, Sputtering
- lift-off: remove resist mask excess film
- finished pattern:

spin-coating

photoresist

substrate

mask plate

contact, projection

UV light
Substrate treatment process

1. Spin-coating
2. Contact or Projection exposure
3. Selective dry/wet etching or doping
4. Remove resist mask
5. Finished pattern
Experimental transistors for future process generations

65nm process 2005 production
45nm process 2007 production
32nm process 2009 production
15nm
10nm

CMOS
0.8 nm conventional gate oxide

22nm process 2011 production

Intel C. Michael Garner
Moore’s Law:
a 30% decrease in the size of printed dimensions every two years
Large circuit functions on a single semiconductor substrate = Reduced cost!

source: Intel

>220M Transistors Integrated into Devices Produced Today
SOURCES OF RADIATION FOR MICROLITHOGRAPHY

Minimum feature size is scaling faster than lithography wavelength. Advanced photo mask techniques help to bridge the gap.

Mark Bohr, Intel
The Ultimates of Optical Lithography

**Resolution:** \( R = k_1 \left( \frac{\lambda}{NA} \right) \)

\( NA = \sin \theta = \text{numerical aperture} \)

\( k_1 = \text{a constant for a specific lithography process} \)

smaller \( k_1 \) can be achieved by 

improving the process or resist contrast

**Depth of Focus** \( \text{DoF} = k_2 \left( \frac{\lambda}{NA^2} \right) \)

Calculated \( R \) and \( \text{DoF} \) values

<table>
<thead>
<tr>
<th>UV wavelength</th>
<th>248 nm</th>
<th>193 nm</th>
<th>157 nm</th>
<th>13.4 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Typical NA</strong></td>
<td>0.75</td>
<td>0.75</td>
<td>0.75</td>
<td>0.25</td>
</tr>
<tr>
<td>Production value of ( k_1 )</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
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<tr>
<td><strong>Resolution</strong></td>
<td>0.17 ( \mu m )</td>
<td>0.13 ( \mu m )</td>
<td>0.11 ( \mu m )</td>
<td>0.027 ( \mu m )</td>
</tr>
<tr>
<td>DoF (assuming ( k_2 = 1 ))</td>
<td>0.44 ( \mu m )</td>
<td>0.34 ( \mu m )</td>
<td>0.28 ( \mu m )</td>
<td>0.21 ( \mu m )</td>
</tr>
</tbody>
</table>

P.F. Carcia et al. DuPoint Photomasks, Vacuum and Thin Film (1999)
Optical Proximity Correction

used in 90 nm (193nm) production line

Drawn structure  Add OPC features  Mask structure  Printed on wafer

Mark Bohr, Intel
Two types of phase shift mask

1. Alternating aperture phase shift mask
   - Amplitude at mask
   - Amplitude at wafer
   - Intensity at wafer
   - 1. dark line appears at the center
   - 2. Applicable only in limited structures

2. Embedded attenuating phase shift mask
   - Absorbing phase-shifter
   - Amplitude at mask
   - Amplitude at wafer
   - Intensity at wafer
   - 6~18% transmittance
   - 1. Can even improve DoF
   - 2. Use MoSi$_2$O$_y$N$_z$, SiN$_x$ or CrO$_x$F$_y$ instead of Cr

Ref: P.F. Garcia et al. DuPoint Photomasks, Vacuum and Thin Film
Material Engineering gains importance!
90 nm Generation Transistor

This is nano technology!

source: Intel develop forum
Spring, 2003
Nano materials will play an important role in the silicon nanotechnology platform

Interconnectors with high electrical conductivity

- Low K interlevel Dielectric
- High K gate oxide
- Strained Si
- Photoresist

Introduction of high-K gate dielectric

90 nm process

- Capacitance: 1X
- Leakage: 1X

Experimental high-K

- Capacitance: 1.6X
- Leakage: <0.01X

Carolyn Block, Intel
A message from Intel

Compress P-doped regions by filling SiGe into carved trenches, hole conduction increased by 25%

Stretch N-doped regions by annealing SixNy cover layer, electron conduction increased by 10%

Strained silicon benefits
- Strained silicon lattice increases electron and hole mobility
- Greater mobility results in 10-20% increase in transistor drive current (higher performance)
- Both NMOS and PMOS transistors improved

# Introduction of new materials

<table>
<thead>
<tr>
<th>1st Production</th>
<th>1997</th>
<th>1999</th>
<th>2001</th>
<th>2003</th>
<th>2005</th>
<th>2007</th>
<th>2009</th>
<th>2011</th>
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<tbody>
<tr>
<td>Process Generation</td>
<td>0.25 μm</td>
<td>0.18 μm</td>
<td>0.13 μm</td>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
<td>32 nm</td>
<td>22 nm</td>
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<tr>
<td>Wafer Size (mm)</td>
<td>200</td>
<td>200</td>
<td>200/300</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>Inter-connect</td>
<td>Al</td>
<td>Al</td>
<td>Al</td>
<td>Cu</td>
<td>Cu</td>
<td>Cu</td>
<td>Cu</td>
<td>?</td>
</tr>
<tr>
<td>Channel</td>
<td>Si</td>
<td>Si</td>
<td>Si</td>
<td>Strained Si</td>
<td>Strained Si</td>
<td>Strained Si</td>
<td>Strained Si</td>
<td>Strained Si</td>
</tr>
<tr>
<td>Gate dielectric</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>High-k</td>
<td>High-k</td>
<td>High-k</td>
</tr>
<tr>
<td>Gate electrode</td>
<td>PolySi</td>
<td>PolySi</td>
<td>PolySi</td>
<td>PolySi</td>
<td>PolySi</td>
<td>Metal</td>
<td>Metal</td>
<td>Metal</td>
</tr>
</tbody>
</table>

*source: Intel develop forum*
Three types of new Fully Depleted Transistors

- SOI wafer
- Planar fully depleted SOI
- Non-planar Double-gate (FinFET)
- Non-planar Tri-gate
Fully Depleted Transistors made on SOI wafers

Non-planar Double-gate (FinFET)

Non-planar Tri-gate

Raised S-D using Selective Epi-Si Deposition

Robert Chau, Intel
From Tri-gate transistors to Nano-wire transistors

depletion electric field

Tri-gate transistor

Nano-wire transistor
Future light sources:

- Extreme UV
- Electron beam
EUV exposure tool

- Uses very short 13.4 nm light
- 13.4 nm radiation absorbed by all materials
- Requires reflective optics coated with quarter-wave Bragg reflectors
- Uses reflective reticles with patterned absorbers
- Vacuum operation
EUV reflective mask

- Mo (~2.8nm)
- Si (~4.1nm)
- 40 Mo/Si pairs
- low thermal expansion
- glass substrate
- Si02 buffer
- Cr absorber
- 13 nm EUV light
- Intel EUV mask
- reticles
EUV mask and patterned resist

Source: Intel
Electron-Beam Lithography

Electron Beam (e-beam) Gun:

Electrons generated by:
- Thermionic emission from a hot filament.
- Field aided emission by applying a large electric field to a filament.
- Or a combination of the two.

Filament is negatively biased (cathode) and electrons are accelerated to the substrate at typically 25 - 100 keV.

\[ eV = \frac{\hbar^2 k^2}{2m_e} \Rightarrow \lambda \approx 0.25 \sim 0.12 \text{nm} \]

E-beam is focused to a small spot size using:
- Electrostatic lenses
- Magnetic fields
- Apertures

A scanned e-beam spot “writes” the image in the resist one “pixel” at a time. X,Y direction of beam is controlled by electrostatic plates.
ELECTRON BEAM LITHOGRAPHY SYSTEM

EOC CONTROL SYSTEM

EXPOSURE CONTROL SYSTEM

EOC CONTROL

STAGE CONTROL SYSTEM

LASER INTERFEROMETER

STAGE CONTROL

CPU

CONTROL IF

VACUUM CONTROL

VACUUM PUMP

X-Y-Z STAGE
ELECTRON OPTICS SYSTEM

TFE electron gun

Acceleration tube

Alignment coil
Blanking electrode
Blanking aperture

Electromagnetic lens

Alignment coil
Objective aperture

Objective lens

ION PUMP

ION PUMP

ION PUMP

Sample stage
Electron Optics

- Acceleration tube
- Blanking electro
  Blanking aperture
- Electromagnetic lens
- Objective aperture
- Objective lens
- X-Y-Z Stage
1st Alignment coil
2nd Alignment coil
Electromagnetic lens
Electrostatic Deflector

1st Electrostatic Deflector

2nd Electrostatic Deflector

Objective lens
Beam spot size vs. beam current for different apertures
Modification of an SEM based e-beam writer

- Blanking circuit
- XY deflection DAC
- SEM internal XY scan signal
- Magnification, etc
- Step motor control
- RS232
- Image ADC
- FARADAY CUP AND GOLD STANDARD
- SAMPLE STAGE INSULATOR
- ELECTRON SOURCE
- BEAM BLANKER
- CONDENSE LENS
- OBJECT LENS APERTURE
- DEFLECTION COILS
- SECONDARY ELECTRON DETECTOR
- PC
- CAD
- Step motor control
Comparison between 30keV and 100keV e-beam writer

1. Good for prototype test
2. Thin resist line-width < 30nm
3. Clear align key image
4. Good for lift-off process
5. Lack of stage stability

1. Good for large area exposure
2. Thin resist line-width < 10nm
3. Require thick/clear align keys
4. Require extra resist engineering
5. Stable/accurate stage stability
Electron beam exposure involves the interaction of primary electrons with a substrate, resulting in the emission of secondary and backscattered electrons. The positive-tone e-beam resist is patterned during the exposure process. After development, the pattern is revealed, and the proximity effect, which can limit resolution, is a main factor to consider.

**Principal of Electron Beam Exposure**

- Electron beam
- Positive-tone e-beam resist
- Substrate
- Backscattered electrons
- Secondary electrons
- Traces of electrons

**After development**

**Proximity effect**: main resolution limiting factor

- Primary electrons
- Backscattered electrons
- Secondary electrons
- Stray exposure
Lift-off and Etching processes

a) PMMA (200~400 nm) substrate
   spin coating + curing

b) electron beam exposure
   braking chemical bonds

c) development

d) O₂ plasma
   clean residual resist

e) deposition
   evaporation from point source

f) lift-off
   remove resist

da) PMMA (200~400 nm) substrate
   spin coating on film

b) electron beam exposure
   braking chemical bonds

c) development

d) reactive ion etching
   dry or wet etching

e) acetone bath
   remove resist
Resist profile made by high energy beam exposure
Controlling undercut in bottom layer resist

- Linewidth 100nm
- Linewidth 70nm
- Linewidth 50nm
- Linewidth 30nm
- Linewidth 20nm
quasi-3D polymer photonic crystal

Transmission spectra, different lattice constants

Frequency ($\omega a/2\pi c$)

Transmission (a.u.)

Wavelength (nm)

400nm

350nm

300nm

random
3D polymer structures

(a) (b)

µm

500nm

1µm

2µm
Examples of 100keV e-beam lithography

3nm NiCr wire

D. R. S. Cumming et al.,
Microelectronic Engineering 30 (1996), 423
Machine: Modified JEOL 100CXII
Kelvin Nanotechnology Ltd

13nm Au wire

M. Kamp et al.
Machine: Eiko E 100

8 nm negative-tone inorganic resist

Machine: 100-keV e-beam writer
NTT Basic Research Laboratories
Sub-10 nm Electron Beam Nanolithography
Using Spin Coatable TiO$_2$ Resists

*University of Cambridge and Leica Microsystems Lithography Limited
Leica VB6-UHR-EWF 100keV*

EB露光装置の用途と方式の違い

研究開発用
スポットビーム方式

半導体生産用
矩形成形ビーム方式と投影方式
Issues related to the integrated circuit industry:

- **Slow throughput**
  - A 0.1 µm diameter beam is $< 10^{-12}$ the area of a 6” wafer.

**Projection EBL Systems (SCALPEL):**

Scattering with angular limitation in projection electron beam lithography
**Multibeam direct-write electron beam lithography system**

Single source with correction lens array

\[ \approx 50 \text{ wafers/hr} \]

Multi-source with single electron optical column

\[ \approx 60 \text{ wafers/hr} \]

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Canon Inc.


Ion Diagnostics Incorporated
Take home message:

Extreme ultraviolet electron beam projection are considered leading contenders for next generation lithography.

However, electron beam direct write system is a maskless lithography.
• eliminating mask amortization costs and
• speed up chip development cycles.

The ultimate resolution of electron beam lithography remains to be explored.

Main applications:
• manufacture of small volume specialty products
• direct write for advanced prototyping of integrated circuits
• studies of quantum effects and other novel physics phenomena at very small dimensions