Effect of Annealing Time on Structure, Composition and Electrical Characteristics of Self-Assembled Pt Nanocrystals in Metal-Oxide-Semiconductor Memory Structures

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Effect of annealing time on structure, composition and memory characteristics of self-assembled Pt nanocrystals from reduction of an embedded PtOx ultrathin film in metal-oxide-semiconductor (MOS) memory structures were investigated in this work. The morphology and dimension of Pt nanocrystals are obviously dependent on the time of annealing in vacuum. It can be seen that the Pt nanocrystals have a narrow size distribution in the range of 2-3 nm and are well separated in SiO2 matrix annealed for 25 and 50 mins. Meanwhile, it clearly exhibits that the nanocrystals contain mainly pure Pt metal along with a slight amount of Pt silicide by X-ray photoelectron spectroscopy. The increase of Pt silicide amount with increasing the annealing time was observed and the almost saturation amount of Pt silicide was found in the device annealed for 50 mins. A significant charge storage effect, a threefold increase of stored charge density and the superior retention characteristic of the device annealed for 50 mins are achieved most likely due to the small lateral charge loss between Pt nanocrystals, and the decrease of the defect injection effect. The magnitude of the hysteresis (ΔVfb, hysteresis) almost remained unchanged at different frequencies, indicating that the C-V hysteresis loop results mainly from the change that is trapped inside the potential well of Pt nanocrystals in SiO2 matrix.

The flash memory is the most widely used nonvolatile memory because it has several advantages such as high density, low manufacturing cost, stable operation 1–3 and so on. However, recently, the scaling-down of the flash memory cell size has become more and more difficult, because the tunneling oxide thickness cannot be scaled down with device size due to the difficulties of keeping the excellent charge retention and endurance characteristics.4 In order to solve this problem, new nonvolatile memories such as Si-nanocrystal memory has been proposed.5–8 Therefore, metal-insulator-semiconductor (MIS) structures based on semiconductor or metal nanocrystals are widely studied for their new physical phenomena as well as their potential applications in nonvolatile memory devices of next generation in recent years, where semiconductor or metal nanocrystals were embedded in the gate dielectric.8–23 In the previous literatures, the performance and characteristics of nonvolatile nanocrystal-floating gate memories are strongly dependent on the control of nanocrystal size, shape, density, distribution and position in the thin gate oxide.5,16,24,25

For example, a new technique in fabrication of the nanocrystals was proposed, which is accomplished through spontaneous decomposition during chemical vapor deposition, by Tiwari et al. in 1996.5,16 The authors demonstrated the use of silicon nanocrystals to replace the floating gate of a conventional memory device. The unique of this method is the shape of the deposited nanocrystals. They are semispheres which expose the largest cross section for tunneling leading to the most efficient injection.5,16 This new nonvolatile memory structure, a metal-oxide-semiconductor structure based on Si nanocrystals, gains the better operating performance. In 2003, the rapid-thermal-annealing effect on the charge loss in MOS capacitors with Ge nanocrystals was demonstrated by Kim et al.24 Therefore, one of the main challenges in the application of nanocrystal memory devices is in the precise control with the structural characteristics of the nano-scaled dots. That is to say, to find a way to control the uniformity of size, density, shape and dispersion of these dots. In general, post-annealing of the semiconductor or metal nanocrystals is an important process in controlling the structural characteristics of the nanocrystal.24,26,27 Some previous literatures have reported effects of annealing on metal nanocrystals made by various processes including chemical vapor deposition, electron beam evaporation, molecular beam epitaxial and chemical solution. However, the effect of annealing on self-assembly Pt nanocrystals from reduction of an ultrathin PtOx layer (called oxide reduction process) has not been reported yet, up till now. Moreover, according to the results in the previous paper,18 the defect injection effect results from the imperfection of sputtered gate oxide. The advantage of this approach (oxide reduction), compared to the surface agglomeration (solid-state dewetting) of Pt nanocrystal by depositing pure Pt, is that the dissipated oxygen atoms can diffuse into the oxide layer of SiO2 to improve the quality of the sputtered oxide in the reduction process. To reduce the defects in the sputtered oxide, the timely annealing process is necessary. In this paper, therefore, we will try to control the size and uniformity of Pt nanocrystals more accurately by using different annealing time in this self-assembly process. The effect of annealing time on the structure, composition and electrical characteristics of the self-assembled Pt nanocrystals in MOS devices will be demonstrated.

Experimental

The MOS device fabrication involves several procedures including RCA substrate clean, dry oxidation, a PtOx ultrathin film and the gate oxide deposition, Pt nanocrystals formation by post-annealing, and metallization. A trilayer structure of the MOS device, containing a thin tunnel oxide layer of thermally-grown SiO2, an ultra thin PtOx layer, and a gate oxide layer of sputtered SiO2, was prepared in sequence. The thickness of the tunnel oxide, PtOx layer and gate oxide are fixed at 2.5 nm, 4 nm and 24 nm, respectively. An ultrathin PtOx film of ~4 nm thick was deposited at room temperature by reactive magnetron sputtering with a low rf power giving a deposition rate of 8 nm/min. The Pt target of 3 inch in diameter was used for the deposition. The sputtering chamber was pumped down to a base pressure of 5*10−5 torr, and then a mixture gas of argon and oxygen was introduced. The total flux of gas is 20 sccm and Ar/O2 ratio is equal to 1/3. Sputtering was performed at the power of 40 W for the PtOx layer, under a working pressure of 20 mtorr. After deposition, all the MOS devices were then annealed in vacuum. To reduce the metallic contamination and nanocrystals with non-uniform size and arbitrary shape, a relatively lower annealing temperature of 425°C that is compatible with the conventional CMOS process was used in this work. Different annealing time of 0.5, 25, and 50 min were used, sequentially. All MOS capacitors were then fabricated by deposition of Pt top electrode (200 μm in diameter) with the hard mask process at 250°C to improve the adhesion between Pt and SiO2. The MOS structure was examined by high resolution transmission electron microscopy (TEM) to observe the morphology and distribution of nanocrystals. According to the analysis of X-ray photoelectron spectroscopy (XPS), the chemical state of the nanocrystals composition can be determined and be
Results and Discussion

Analyses of structure and composition of self-assembled Pt nanocrystals from reduction of an embedded PtOx ultrathin film.— The MOS structure devices with embedded Pt nanocrystals are formed after post annealing in vacuum and each metal nanocrystal acts as a small floating gate. In these devices, even if a charge leakage path exists between the small floating gate and the substrate, the control gate or another small floating gate, only a small part of charges stored in the Pt nanocrystals is lost. Accordingly, the effect of the morphology and distribution of Pt nanocrystals on the charge storage and retention characteristics of this new nonvolatile memory device is interesting and worthy of note. The illustration of cross-sectional and plane-view images of transmission electron microscopy in Figure 1 shows the annealing time effect on Pt nanocrystals formation in SiO2 matrix. Figure 1a, 1d, 1b, 1e, and 1c, 1f shows that as-deposited PtOx films were reduced to form Pt nanocrystals after annealing in vacuum at 425°C for 5, 25, and 50 mins, respectively. As shown in Figure 1a and 1d, the chemically unstable PtOx layer18,28 can be decomposed at 425°C in vacuum to form an irregular island pattern of Pt with oxygen dissipation. For a long enough annealing time (25–50 mins) at 425°C, when the PtOx film is annealed to give the atoms enough surface mobility, the film will self-assemble into a low-total energy state. Therefore, the spherical Pt nanocrystals were formed because of surface energy minimization.22 In Figure 1b and 1e for the device annealed for 25 mins, discrete Pt nanocrystals in SiO2 matrix were mostly spherical with a average size distribution in the range of 2.0–2.5 nm and the spacing among two Pt nanocrystals is short with a distance in the range of less than 10 nm. The well-isolated Pt nanocrystals with a average size distribution in the range of 2.5–3.0 nm are formed after annealing at 425°C for 50 mins as shown in Figure 1c and 1f. Note that the average size of nanocrystals in Figure 1c is larger than that in Figure 1b due to the longer segregation and diffusion time. In conclusion, as a result of TEM investigations, the morphology and dimension of Pt nanocrystals are obviously dependent on the time of annealing in vacuum. It can be seen that the Pt nanocrystals have a narrow size distribution in the ranges of 2-3 nm and are well separated in SiO2 matrix annealed over 25 mins. Also, a very high density (larger than 2*10¹² cm⁻²) of the Pt nanocrystals, was obtained in the devices annealed over 25 mins. It may be worth pointing out, in passing, that it is easier to produce such a small and uniform dimension distribution of metal nanocrystal by using this self-assembly process than by using an E-beam writer. For the further analysis, the crystalline nature of the Pt nanocrystals is also evidenced in the cross-sectional HREM image shown in Figure 2. The lattice image of the Pt nanocrystals confirms the reduction of the amorphous PtOx layer. According to the estimated result of lattice image of Pt nanocrystals, the d spacing (∼0.24 nm) corresponds to that of Pt (111).

The reduction of the PtOx layer was found to be sensitive to the annealing time in this work. Figure 3 shows the XPS spectra of Pt 4f electrons for the PtOx layer annealed in vacuum for different time. According to the data of curve fitting, the binding energies for Pt 4f electrons peaks are found to be around 71.0 eV and 72.3 eV. The binding energies around 71.0 eV should correspond to metallic Pt (71.1 eV)18,28,29 but those of ∼72.3 eV could correspond to PtOx or PtSi (72.2–72.5 eV).18,28–30 However, platinum oxides (PtO and PtO2) aren’t chemically stable and can be easily reduced back to metallic state, Pt, at above 400°C in vacuum.28 Besides, an increase of the amount of the unknown compound at ∼72.3 eV with increasing the annealing time from 5 to 50 min was observed as shown in Table I. For the reasons given above, the unknown compound at ∼72.3 eV could be Pt silicides not oxides.18,28–30 As shown in Figure 3a, all platinum oxides have been already transferred into metallic platinum after post-annealing of even only 5 mins. At the same time, platinum silicides were formed by the reaction between metallic Pt and Si dangling bonds.

Table I. Effect of annealing time on the composition ratio of Pt metal to Pt silicide.

<table>
<thead>
<tr>
<th>Annealing time (mins)</th>
<th>Composition ratio of Pt metal to Pt silicide</th>
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<tbody>
<tr>
<td>5</td>
<td>76/24</td>
</tr>
<tr>
<td>25</td>
<td>73/27</td>
</tr>
<tr>
<td>50</td>
<td>72/28</td>
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Figure 2. HREM lattice image of isolated Pt nanocrystals in SiO2 matrix after annealing at 425°C for 25 mins.

Figure 1. Cross-sectional and plane-view TEM images of Pt nanocrystals in SiO2 matrix for different annealing time (a), (d) 5 mins, (b), (e) 25 mins, and (c), (f) 50 mins.
Figure 3. XPS spectra of Pt 4f electrons in reduced PtOx for different annealing time (a) 5 mins, (b) 25 mins and (c) 50 mins. Solid and empty circles indicate experimental and fitting results, respectively.

bond in the surrounding SiO₂ during annealing of 425°C. It clearly exhibits that the nanocrystals contain mainly pure Pt metal along with a slight amount of Pt silicide. The Pt nanocrystals are undoubtedly self-assembled to form from the reduction of the chemically unstable PtOₓ and, subsequently, the segregation of the reduced product, Pt, in the matrix of SiO₂ at high temperature. Meanwhile, a slight increase of Pt silicide amount with increasing the annealing time was observed as shown in Table I. The almost saturation amount of Pt silicide generated at the interface between SiO₂ matrix and nanocrystals was found in the device annealed at 425°C for 50 mins. Therefore, the Pt silicide was reasonably judged in the position of the outside shell of nanocrystals.

Effect of annealing time on memory characteristics of Pt nanocrystals in MOS devices with a fixed 2.5 nm-thick tunnel oxide.— The charge storage effect is the most important characteristics of the nanocrystal in MOS capacitors. Hysteresis in C-V relations corresponding to forward and reverse voltage sweeps is the evidence for charge storage in nanocrystal memory devices. The MOS devices were thus fabricated with Pt top electrode (200 μm in diameter) deposited and patterned by hard mask. The typical high frequency (1 MHz) C-V relations in the MOS devices with or without embedded Pt nanocrystals were measured with the voltage swept from accumulation to inversion and back, and exhibited in Figure 4. The reference device without Pt nanocrystals shows a negligible C-V hysteresis loop. However, there is a clear negative $V_{FB}$ shift appearing in the C-V curve of the reference sample, indicating the presence of the positive fixed charges in the MOS structure. In contrast, the Pt-nanocrystal-embedded MOS device annealed for 50 mins exhibits a broad hysteresis loop in the C-V relations accompanied by a large flatband voltage shift, $\Delta V_{FB}$ (referred as the memory window), suggesting the significant charge storage effect. It should be noted that the direction of C-V hysteresis loop is counterclockwise and is related to the substrate injection of charges into the nanocrystals. Moreover, the center of the hysteresis loop of the specimen containing Pt nanocrystals is located close to the zero gate voltage, suggesting that the positive fixed charges in the MOS structure are compensated by the negative charges stored in the Pt nanocrystals. Table II summarizes the effect of annealing time (5, 25 and 50 mins) on the charge storage of the devices with embedded Pt nanocrystals. The memory windows ($\Delta V_{hysteresis}$) and estimated densities of the stored charge ($Q_s$) in the three devices annealed for different annealing time are listed in Table II. Then, the estimated densities of the injected charge (hole) at negative gate voltage and the injected charge (electron) at positive gate voltage are divided and also listed in Table II. A threefold increase of stored charge density is achieved with increasing the annealing time from 5 to 50 mins probably due to the small lateral charge loss between Pt nanocrystals, and the decrease of the defect injection effect, which apparently result

<table>
<thead>
<tr>
<th>Annealing time (mins)</th>
<th>$\Delta V_{hysteresis}$ (memory window)</th>
<th>$Q_s$ (carrier /cm²) at negative gate voltage</th>
<th>Injected charge (electron) at positive gate voltage</th>
<th>Direction of hysteresis</th>
</tr>
</thead>
<tbody>
<tr>
<td>05  2.48 V</td>
<td>2.19 × 10¹²</td>
<td>1.4 × 10¹²</td>
<td>0.8 × 10¹²</td>
<td>Counterclockwise</td>
</tr>
<tr>
<td>25  5.44 V</td>
<td>4.86 × 10¹²</td>
<td>1.9 × 10¹²</td>
<td>3.0 × 10¹²</td>
<td>Counterclockwise</td>
</tr>
<tr>
<td>50  6.48 V</td>
<td>5.81 × 10¹²</td>
<td>2.6 × 10¹²</td>
<td>3.2 × 10¹²</td>
<td>Counterclockwise</td>
</tr>
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</table>
of fixed defects, the charge stored in the Pt nanocrystals depends on the difference between the injection-in of electron from substrate and the injection-out of electron to defects. Inversely, under accumulation bias condition, the relative positions of Fermi levels and trap states become reversed, thus, it is determined by difference between the injection-out of electron to or injection-in of hole from substrate and the injection-in of electron from defects.

Once the electrons tunnel into the Pt nanocrystals, they could be trapped inside the potential well of Pt nanocrystals or/and at the interface state between Pt nanocrystals and the SiO2 matrix. The frequency dependence of flatband voltage is related to the trapping stability of electrons in the Pt nanocrystals. The effects of measurement frequency on the flatband voltage shift of C-V hysteresis ($\Delta V_{fb, hysteresis}$) in the devices annealed for different time are plotted in Figure 6. It is clearly observed that the magnitude of the hysteresis ($\Delta V_{fb, hysteresis}$) almost remained unchanged at different frequencies. A similar phenomenon in Si nanocrystal system has also been presented by Huang et al. and Dai et al. Since the interface state is strongly sensitive to the measurement frequency, the hysteresis results mainly from the change that is trapped inside the potential well of Pt nanocrystals in SiO2 matrix, indicating that the charge trapping at the interfaces of the nanocrystals with the oxide matrix is less likely to be the dominant charge storage mechanism.

Charge retention characteristics of the Pt nanocrystals in the above three devices were then measured at room temperature using a ±8 V gate voltage stress for 10 seconds. Figure 7 shows the change of flatband voltage after write (charging) or erase (discharging) with duration time. The flatband voltage window of the three devices

![Figure 5](image)

**Figure 5.** (a) Schematic and (b) modified band diagram of the MOS device with 2.5 (or 5.0) nm-thick tunnel oxide, applied positive gate voltage under inversion condition. (The symbol of red star denotes the fixed defect or trap state in the sputtered oxide.)

from the recovery of defects in the sputtered gate oxide. Moreover, all of the three hysteresis loops in these devices are counterclockwise.

In the previous literature, it is clear that there are two mechanisms of the charge storage effect in the MOS devices with embedded Pt nanocrystals. One is denoted by the counterclockwise hysteresis from substrate injection, and the other is characterized by the clockwise hysteresis attributed to the defect injection from the overlaid sputtered gate oxide. These two mechanisms coexist at the same time but compete with each other. For tunnel oxide being thin enough (<5.0 nm) such as the above device annealed for 50 mins, the defect injection would be significantly suppressed, and thus the substrate injection becomes dominant. The modified schematic of charge storage effects in this MOS device applied positive gate voltage under inversion condition is demonstrated in Figure 5a. When a positive gate bias is applied, the trapping of electrons from the substrate channel into the nanocrystals is easier to happen than the de-trapping of electrons from the nanocrystals to defects. The totally negative charges stored in the Pt nanocrystals lead to the shift of the flatband voltage toward the positive voltage direction. When the gate bias is reversed, the net positive charges captured by the Pt nanocrystals give rise to the shift of flatband voltage to the other direction. Therefore, it leads to the counterclockwise hysteresis loop in the C-V relations for the device annealed for 50 mins. According to the above discussion, the modified band diagram for the MOS device with embedded Pt nanocrystals is proposed in Figure 5b. As depicted in Figure 5b, under inversion bias condition which gives the Fermi level of Pt nanocrystals lower than that of substrate but higher than the trap state
significantly narrows within 10^3 seconds, and becomes stabilized for longer duration. Among them, the device with Pt-nanocrystals prepared by annealing for a longer time has a substantially larger window of after stabilization, i.e., 1.2 V, 0.7 V and 0.3 V for the annealing time of 50 mins, 25 mins and 5 mins, respectively. It reveals the relatively stable characteristic of charge storage in the devices. The superior retention characteristic of the device after annealing for 50 mins is most likely due to (1) the small lateral charge loss between Pt nanocrystals, and (2) the recovery of defects in the sputtered oxide to decrease the defect-assisted leakage.

Conclusions

Metal-oxide-semiconductor memory structures based on Pt nanocrystals were successfully fabricated from the reduction of an ultrathin PtOx layer. Effect of annealing time on the structure and memory characteristics of self-assembled Pt nanocrystals in SiO2 matrix was studied. The morphology and dimension of Pt nanocrystals are obviously dependent on the time of annealing in vacuum. For a long enough annealing time (over 25 min), the Pt nanocrystals are not only well isolated but also uniformly dispersed. According to the composition analysis by the XPS spectra of Pt 4f electrons, the reduction of the PtOx layer was also found to be sensitive to the annealing time. It clearly exhibits that the nanocrystals contain mainly pure Pt metal along with a slight amount of Pt silicide. The MOS structure embedded with Pt nanocrystals exhibits a broad hysteresis loop in the C-V relations that is accompanied by a large flatband voltage shift, thereby revealing a significant charge storage effect. A threefold increase of stored charge density and the superior retention characteristic of the device annealed for 50 mins are most likely due to the small lateral charge loss between Pt nanocrystals, and the decrease of the defect injection effect. Moreover, the magnitude of the hysteresis (ΔVfb, hysteresis) almost remained unchanged at different frequencies, suggesting that the C-V hysteresis loop is not due to interface states in the Pt nanocrystal memory device.

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